Optimized RF board layout for STM32WL Series

Introduction

The STM32WL Series microcontrollers integrate RF transceiver for LPWAN (long-power wide-area network), compatible with LoRa®, GFSK, DBPSK, and MSK, in the frequency range 150 to 960 MHz.

The STM32WL Series devices (named STM32WL later in this document) have two output powers:

- HP (high-power RFO_HP), optimized up to 22 dBm
- LP (low-power RFO_LP), optimized up to 15 dBm

The devices also include a differential RF input (RFI, up to 0 dBm) for the Rx low-noise amplifier (LNA).

To achieve the right performances for the RF output and RF input signals, some recommendations must be followed for the board design. Special care is required for the layout of an RF board compared to a conventional circuit.

This document describes precautions to be taken to achieve the best RF performance of the STM32WL on efficient applications, that last for long time under battery. The description is based on the UFBGA73 (5 x 5 mm) reference 4-layer board.

1 Main rules summary

Some general guidelines when routing an RF PCB are listed below:

- RF traces must be short and straightforward.

  Make the transmission lines short and straightforward in order to avoid reflections, save power and reduce high-frequency issues.
- Place and route decoupling capacitors and RF components first.

  The placement of the RF part at first, is highly recommended. Decoupling capacitors are essential to avoid high-frequency problems and maintain power integrity. Do not hesitate to add some other decoupling capacitors if needed.
- Place and route critical signals.
- Do not route high-frequency signals on board outline.

  High-frequency signals on board outline tend to radiate due to edge effects of high-frequency fields.
- Try to maintain the characteristic impedance (50 Ω) constant.

  Avoid discontinuities such as different sizes of pads put on transmission lines, bends, T-junctions, changing RF trace width along the line.
- Keep critical signals away from RF.

  High-frequency signals can induce some undesired effects in critical signals such as electric and/or magnetic coupling.
- For high-frequency applications, 4-layer PCBs are better than 2-layer.
- Try to avoid vias with RF signals.

  Vias in RF paths can cause reflections, radiation and consequently losses.
- RF return current paths must be free of obstacles or discontinuities.
- Avoid undesired magnetic coupling between inductors by leaving space between them, using magnetic shielding and/or placing them perpendicular to each other.
- Try to reduce undesired parasitic capacitances and inductances associated with the circuit layout as much as possible.
- For filter inductors such as SMPS chokes, use shielded inductors to minimizing noise and place them perpendicular to LNA traces and other RF traces.
- To reduce electromagnetic undesired emission, a metal shield can be added above RF components.

This application note applies to STM32WL Series microcontrollers based on the Arm® Cortex®-M processor.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Characteristic and controlled impedance

All transmission lines below microwave frequencies have at least two conductors:

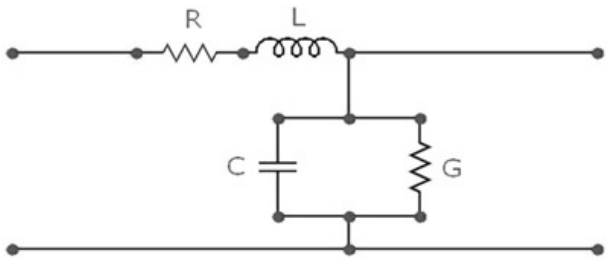
- In one conductor, the RF currents go towards the antenna.
- In the other, the RF currents come back to the RF source.

In order to feed an antenna, transmission lines on PCBs, designed considering their characteristic impedances, are used.

The characteristic impedance of a transmission line (sometimes represented by Z_C or Z_0) is defined as the constant ratio between the voltage and current waves along the line. Z_C can be defined with R, L, G, and C parameters that represent the transmission line model of an extremely short segment, as shown in this formula:

$$Z_C = \sqrt{\frac{R + jwL}{G + jwC}} = \sqrt{\frac{Z_{series}}{Y_{shunt}}}$$

Figure 1. Equivalent circuit of transmission line



Where:

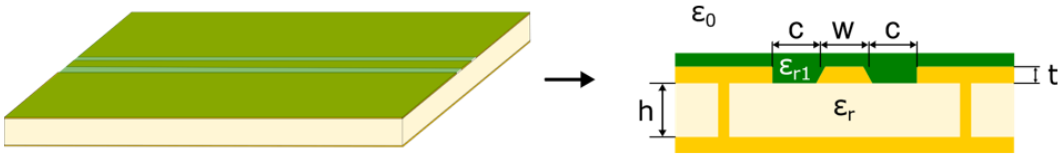
- R = total series resistance, per unit length of two conductors, in ohms
- L = total series inductance, per unit length of two conductors, in henrys
- G = shunt conductance between two conductors per unit length, in siemens
- C = shunt capacitance per unit length between conductors, in farads
- j = imaginary number
- ω = angular frequency, in rad/s

The impedance formed by a PCB trace and its associated reference planes, constitute the characteristic impedance of the transmission line on the PCB. This characteristic impedance on PCBs is frequently called controlled impedance.

To make it simpler, the controlled impedance of a PCB is the physical dimensions that define the R, L, G, and C parameters. Characteristics of the materials, like permeability of permittivity, impact the value of the controlled impedance. Since no magnetic materials are used in PCBs, the relative permeability is considered equal to one ($\mu_r = 1$).

In the example of a coplanar single-ended waveguide line with lower-ground plane (GCPW for grounded coplanar waveguide), the physical dimensions like t (thickness), w (width), c (clearance), h (height) and permittivity constants of dielectric materials, determinate the characteristic impedance of the transmission line on the PCB.

Figure 2. Example of a GCPW in a 2-layer PCB



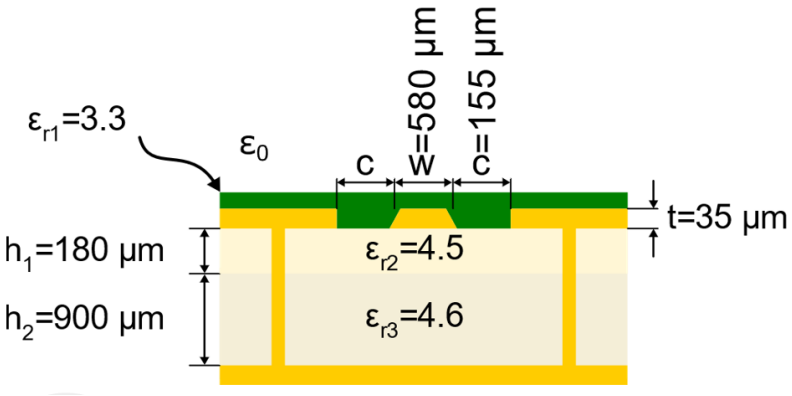
Transmission lines on PCBs can also be made in other formats like microstrip or strip lines.

GCPW is often selected up to a few GHz in order to reduce radiation due to fringe fields, therefore causing less EM (electromagnetic) radiation thus less interference. For STM32WL reference boards, GCPW are used as standard transmission line structures.

GCPW is more sensitive to PCB manufacturing variations than microstrip lines. GCPW physical dimensions (such as t, w, c, and h) must be kept within low tolerances in order to maintain an impedance very close to 50 Ω.

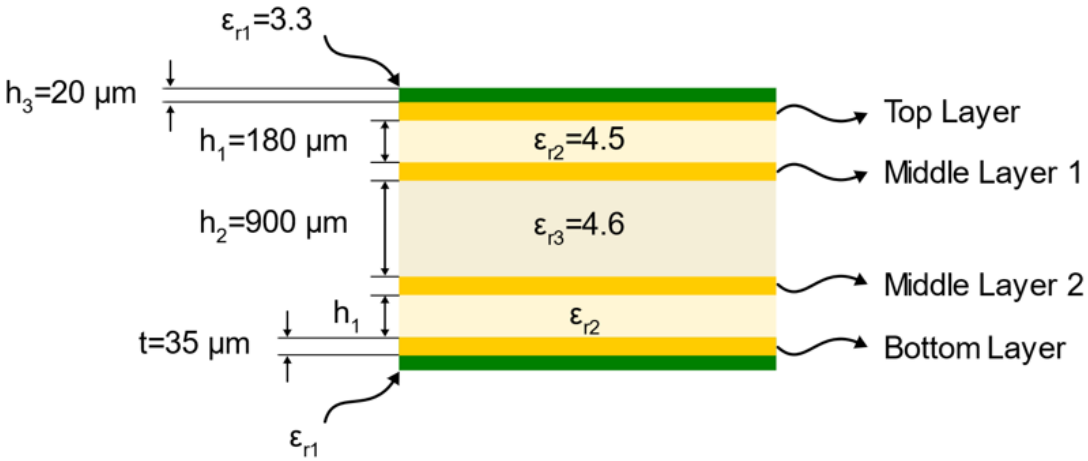
In order to understand how the manufacturing process can impact the characteristic impedance of a GCPW transmission line on a PCB, consider the example of a 4-layer PCB with physical dimensions varying with 20% tolerance, around a 50 Ω characteristic impedance at 1 GHz. In that case, the stack-up with nominal values is shown in the figure below.

Figure 3. Example of a transmission line type GCPW on PCB



The entire PCB stack-up for this example is depicted in the figure below.

Figure 4. Stack-up example for 4-layer PCB



Note: Due to mechanical constraints, PCBs are often made with symmetrical stack-ups.

As the transmission width varies during the manufacturing process within a 20% tolerance, the expected result is shown in the figures below.

Figure 5. Characteristic impedance versus width variation

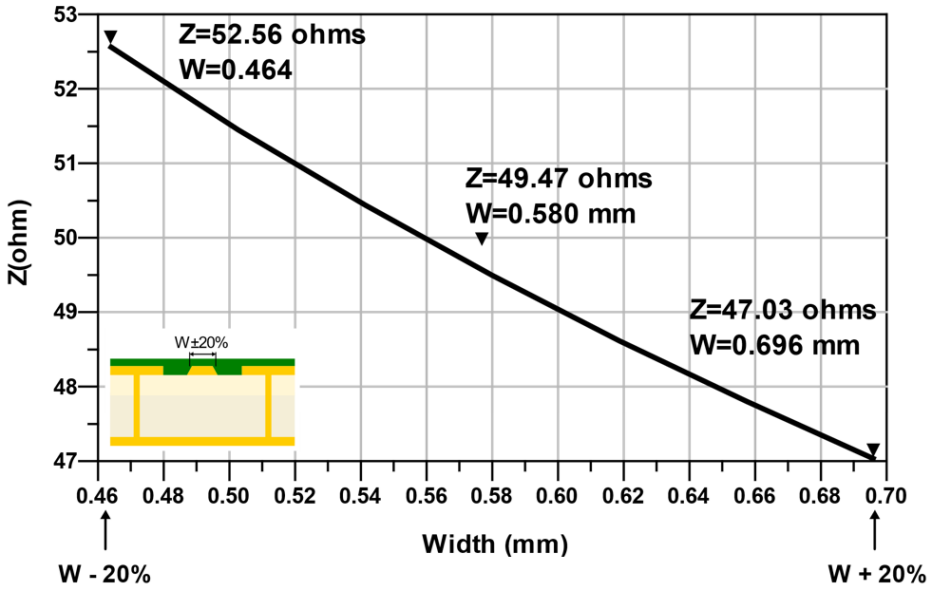
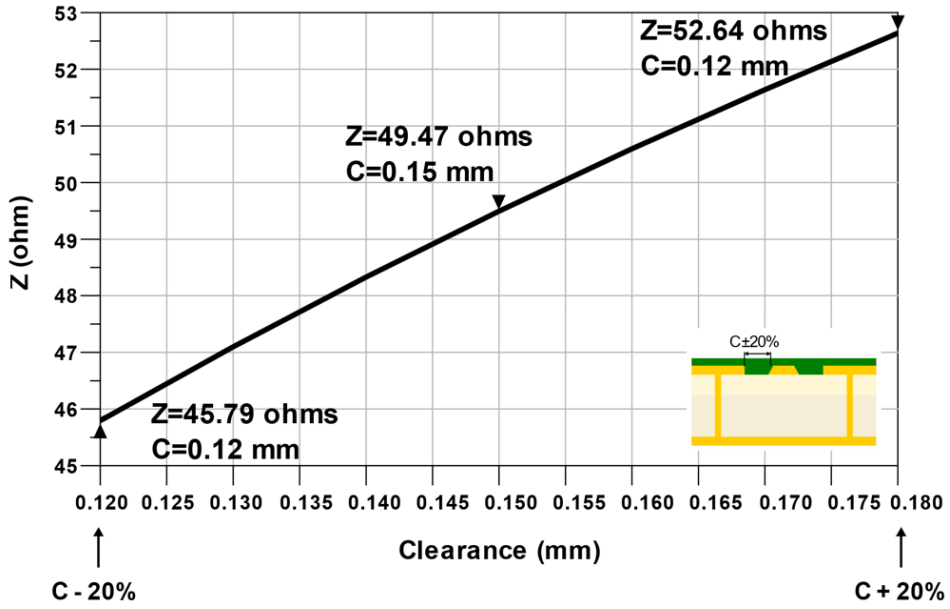
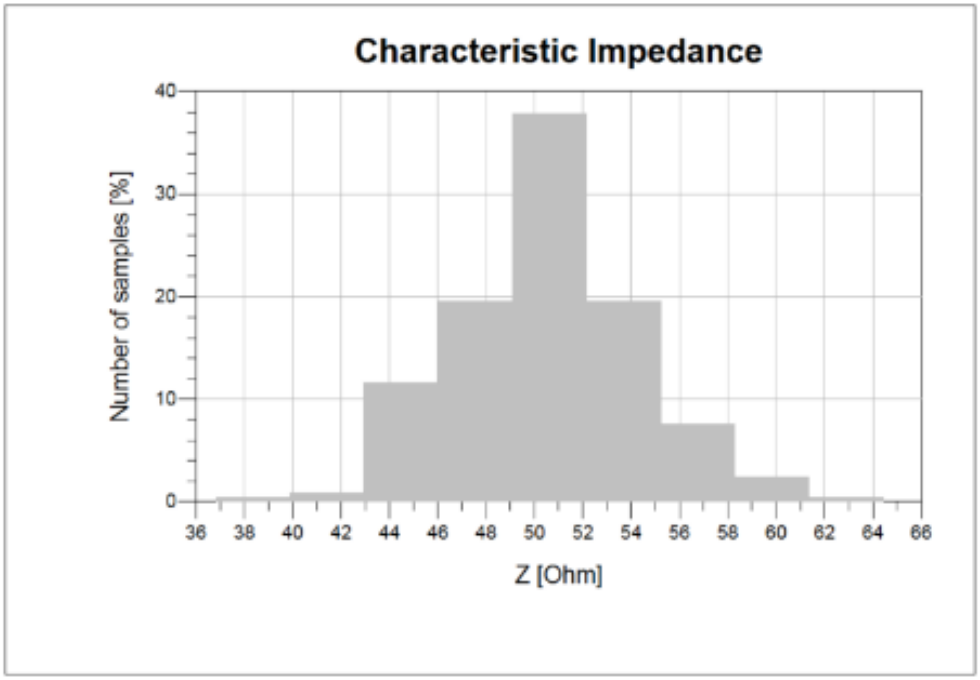


Figure 6. Characteristic impedance versus clearance variation



As explained before due to process fabrication PCBs can have variations in many parameters as dielectric constant, track width, core, and prepreg dimensions. A histogram gives you a main idea of the impedance variation per PCB unit in a fabrication process.

Figure 7. Histograms from statistical analysis for ± 10 % of processes variation of dimensional variables (n = 1000) from ADS



This figure shows the histogram of 1000 PCBs units, which is described as follows:

- 380 have impedance between 49-52 Ω
- 200 have impedance of 46 to 43 Ω
- 200 have impedance between 52-55 Ω
- 60 have impedance of 55 to 58 Ω
- 20 have impedance of 58 to 61 Ω
- etc.

The goal is to design, in theory, transmission lines that can delivery to the antenna 100% of the power inserted at the beginning of the line. To better understand the impact of the mismatch due to a characteristic impedance other than 50 Ω, see the table below.

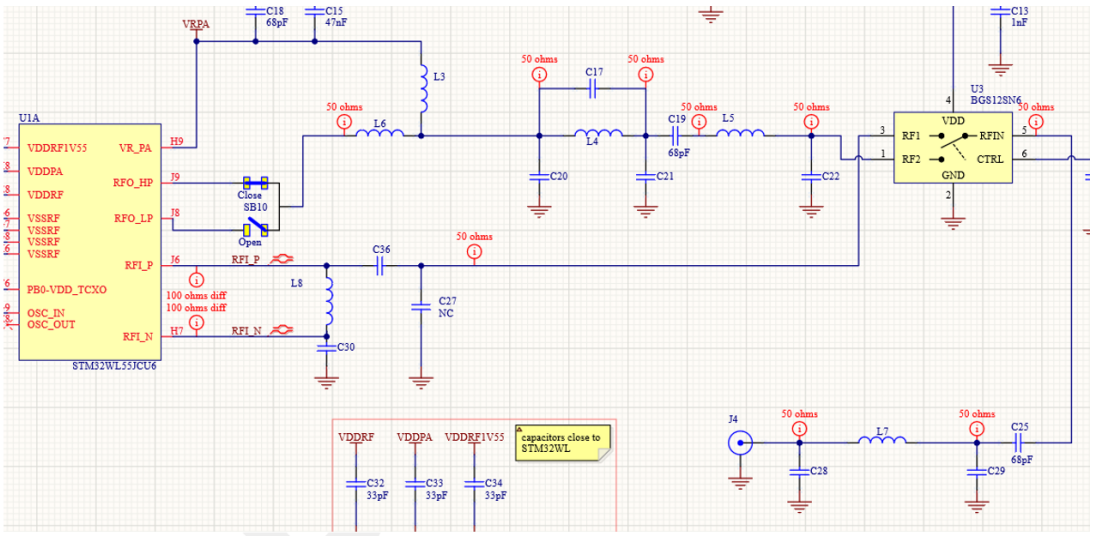
Table 1. Characteristic impedance and impact on RF measures (load impedance = 50 Ω)

Characteristic impedance (Ω)	Reflection coefficient	Return loss (dB)	Mismatch loss (dB)	VSWR(1)	Reflected power (%)	Transmitted power (%)
55	-0.048	0.010	26.444	1.100	0.23	99.77
54	-0.038	0.006	28.299	1.080	0.15	99.85
53	-0.029	0.004	30.714	1.060	0.08	99.92
52	-0.020	0.002	34.151	1.040	0.04	99.96
51	-0.010	0.000	40.086	1.020	0.01	99.99
50	0.000	0.000	-	1.000	0.00	100.00
49	0.010	0.000	39.913	1.020	0.01	99.99
48	0.020	0.002	33.804	1.042	0.04	99.96
47	0.031	0.004	30.193	1.064	0.10	99.90
46	0.042	0.008	27.604	1.087	0.17	99.83
45	0.053	0.012	25.575	1.111	0.28	99.72

1. *Voltage standing wave ratio.*

As a good practice, always identify the controlled impedances in schematics as depicted in the figure below.

Figure 8. Example of schematic with controlled impedance identified



3 RF transmission line

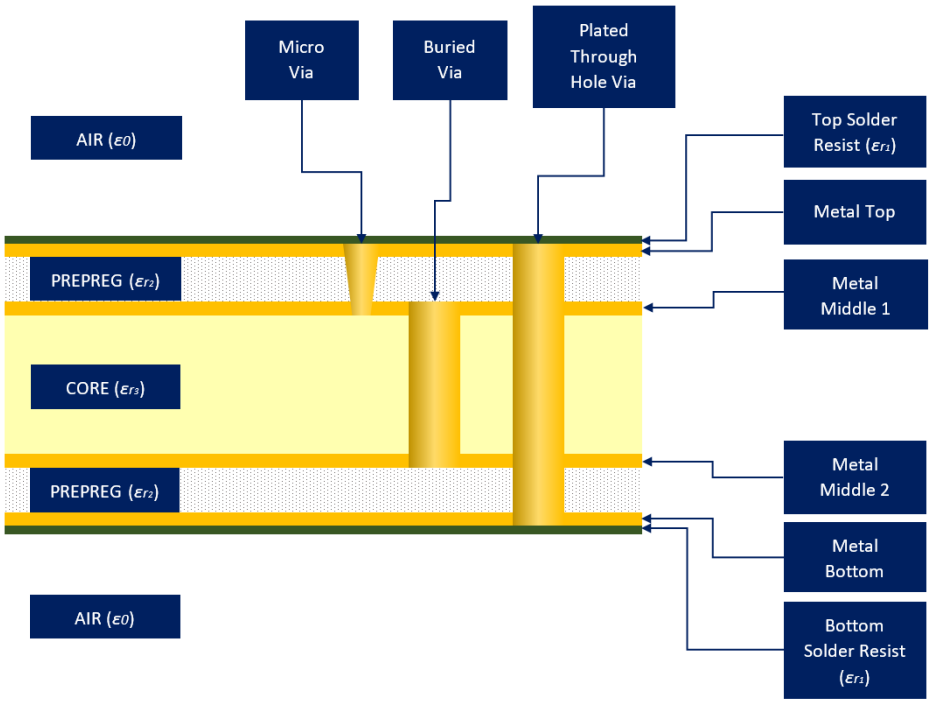
The geometry of a transmission line is defined to minimize the tendency of the line to act as an antenna and to radiate on its own, while the geometry of an antenna is selected to maximize its tendency to radiate.

As mentioned before, the RF transmission line on PCB is defined by its geometry and the PCB stack-up. This section includes a PCB stack-up description and some stack-ups to be copied in order to have the right impedances for the Tx and Rx paths.

3.1 Stack-up board

A typical 4-layer PCB with three types of vias is described in the figure below. The trace width, the distance between trace and ground reference, and the material characteristics determine the impedance of the RF trace. Microvias are often used with BGA packages due to the high-density interconnections (HDI).

Figure 9. Typical 4-layer PCB stack-up with three different types of vias



3.2 Stack-ups for Tx 50 Ω and Rx 100 Ω

One of the most difficult tasks is to correctly determine the width and clearance for an RF track from a given stack-up. The difficulty in linked to the effective dielectric constant (ε_{r_eff}) calculation for a given substrate.

A 2.5/3D field-solver software is often used to determine ε_{r_eff}. PCB manufacturers can assist greatly in this task. Whenever possible, ask to the PCB manufacturer, the design rules (dimensions) to use on the RF lines to obtain 50 Ω single-ended and 100 Ω differential. Otherwise, copy/paste a predefined board stack-up with its characteristics and use the recommended design rules to obtain the desired impedances.

Appendix A Stack-up examples details some stack-up boards to obtain 50 Ω for Tx lines and 100 Ω for Rx lines that can be copied to the application. Contact the PCB manufacturer to verify if the values on the stack-up selected can be guaranteed.

4 Surface mounted components with RF signals

4.1 Capacitors

The table below gives some recommendations regarding the routing of SMD (surface mounted components).

Table 2. Reducing parasitic inductance of routed capacitors

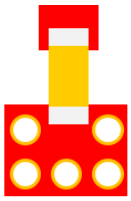
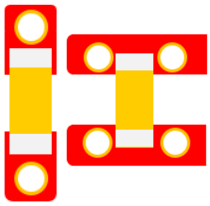
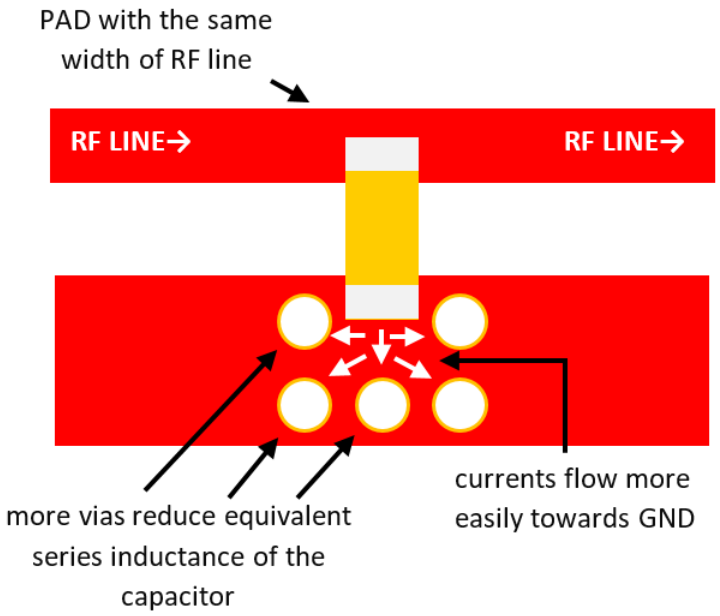
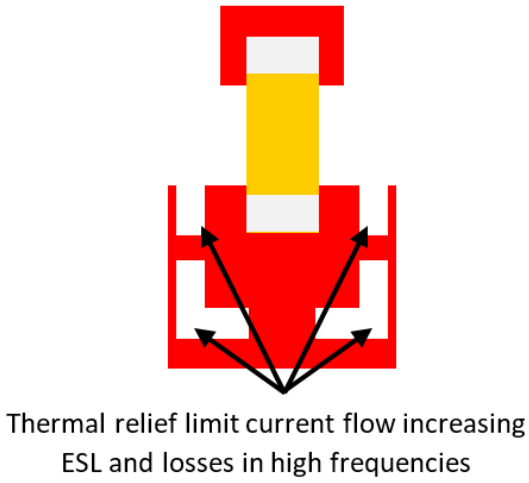
Performance	Capacitor pad type	Comment
Recommended		Short traces with multiples vias reducing return current impedance
Better		Short traces
Better		
Poor		Long traces between capacitor increasing series inductance
Not good		Thinner access track increasing the equivalent series inductance of the capacitor

Figure 10. **Example of capacitors on RF lines**



Whenever possible, thermal reliefs must be avoided on RF lines as they increase the equivalent series inductance (ESL) of capacitors and then change the frequency response of the capacitors in addition to increasing losses.

Figure 11. **Thermal reliefs**



4.2 Inductors

The table below gives some recommendations regarding the inductors.

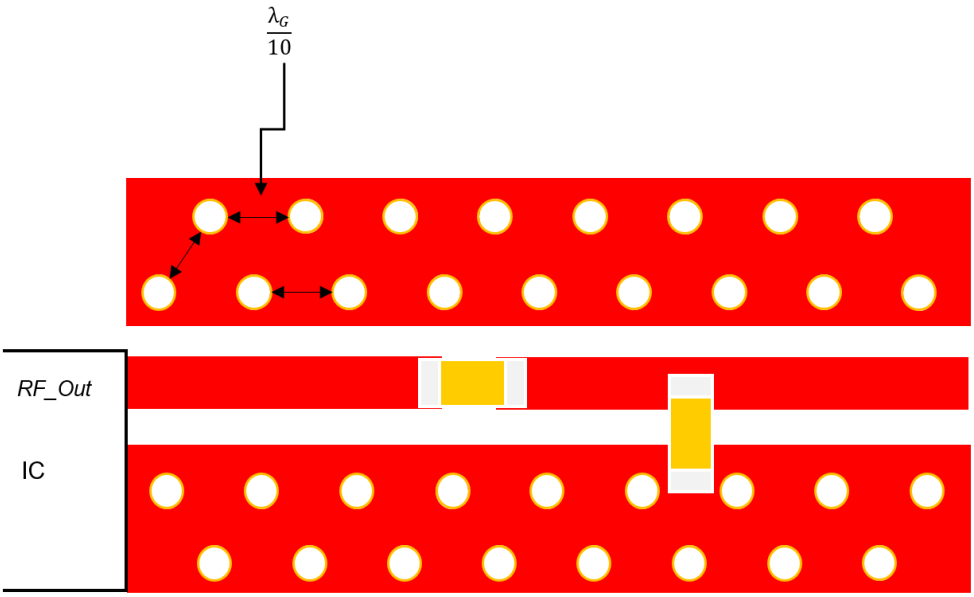
Table 3. Inductor pads with RF signals

Performance	Inductor pad type	Comment
Recommended		Short and same PAD width access traces, maintaining the original value of the inductance and Q-Factor
Not good		Be careful with this kind of tricks. This narrow trace contributes to increase the inductance, but this can decrease the equivalent Q-factor of the inductor. RF inductors are carefully made to have a high Q-factor. Do not ruin it.

5 Via stitching and shielding

The recommendation is to put some vias around RF lines as shown in the figure below, in order to reduce high-frequency issues.

Figure 12. Spacing between vias around GCPW



The following formula is used to determine the D value:

$$\frac{\lambda_G}{20} \leq D \leq \frac{\lambda_G}{10}$$

with λ_G, as guided wavelength, defined by this formula:

$$\lambda_G = \frac{3 \times 10^8}{f \times \sqrt{\epsilon_{r_eff}}}$$

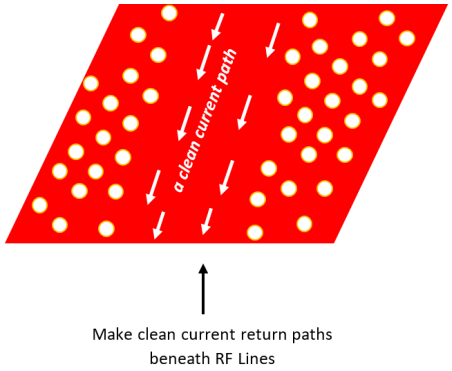
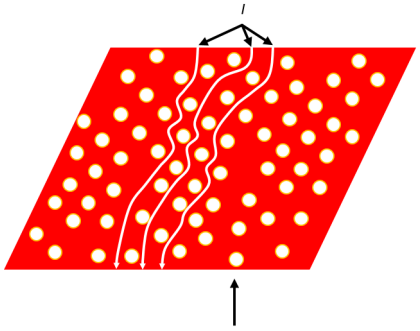
where:

- f = highest frequency of the RF circuit operation
- ε_{r_eff} = effective dielectric constant of the PCB

6 RF return current path

The RF currents that go to the antenna must come back to their source inside the chip to complete a closed loop: it is done by a return path. Thus, a return path for the delivery medium back to the energy source must be provided. A return path is defined as the conductive path taken by the current returning to the source from the load, generally this return path is done on a grounded plane.

Table 4. Return paths

Performance	Return path type	Comment
Recommended		No vias in RF return path
Not good		Vias creating larger RF return path increasing losses and discontinuities

Slots on return path increase impedance, losses and can act as antennas. Slots are not allowed on return path:

Figure 13. Slots on return path

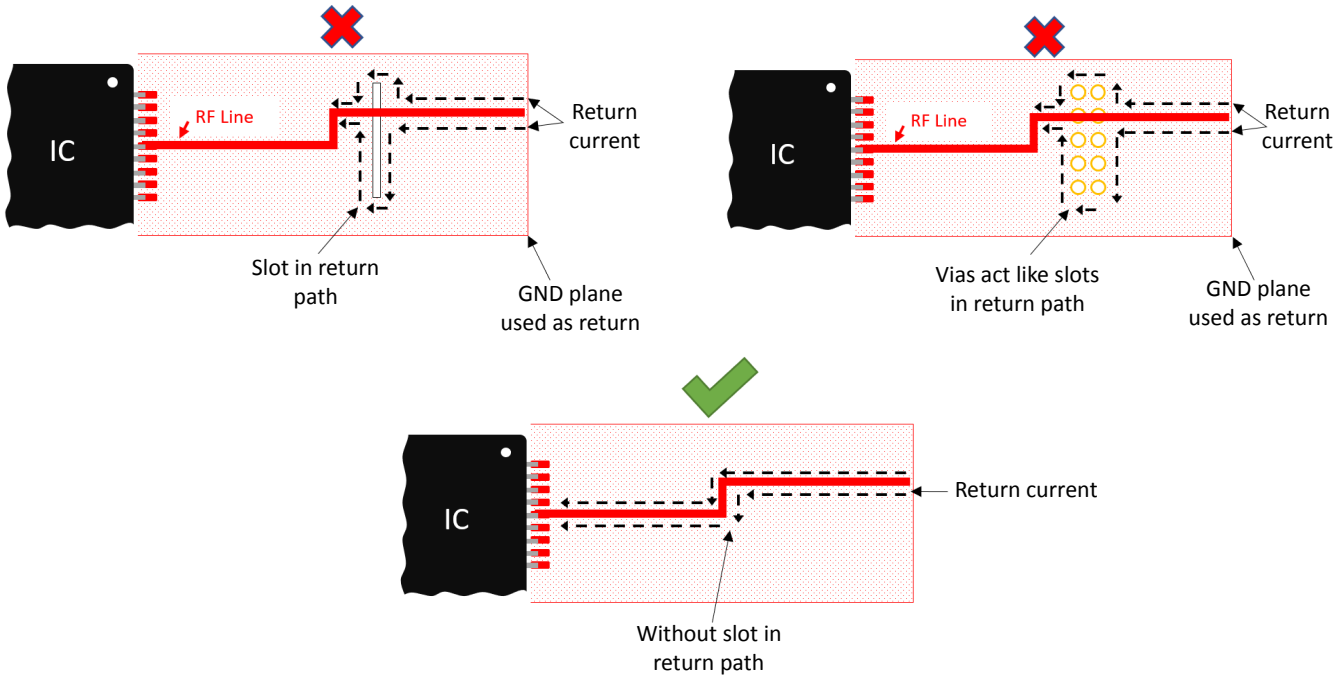
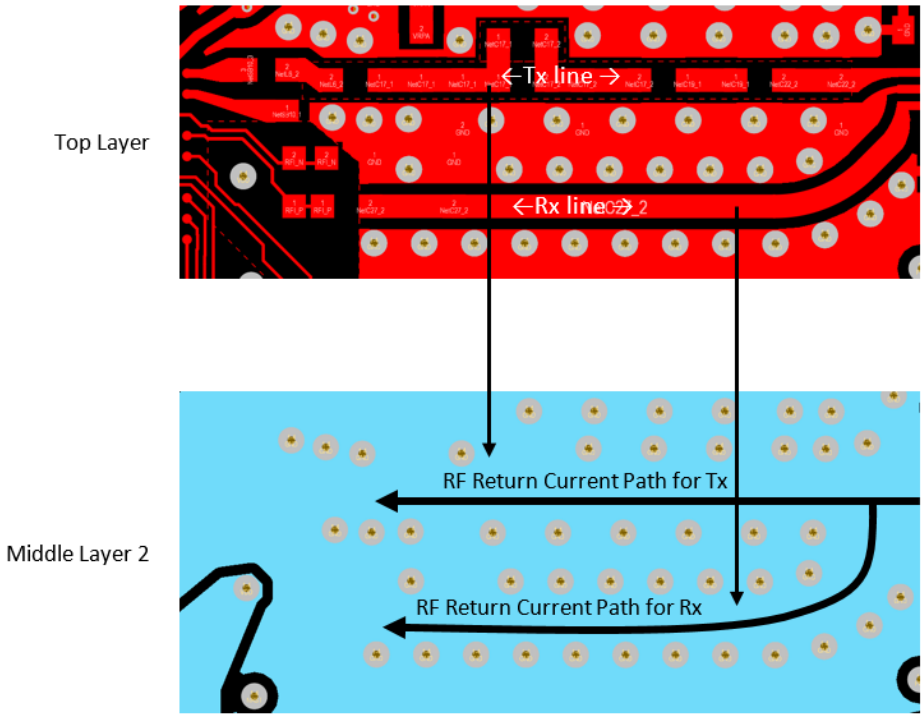


Figure 14. Clean return path example for RF currents

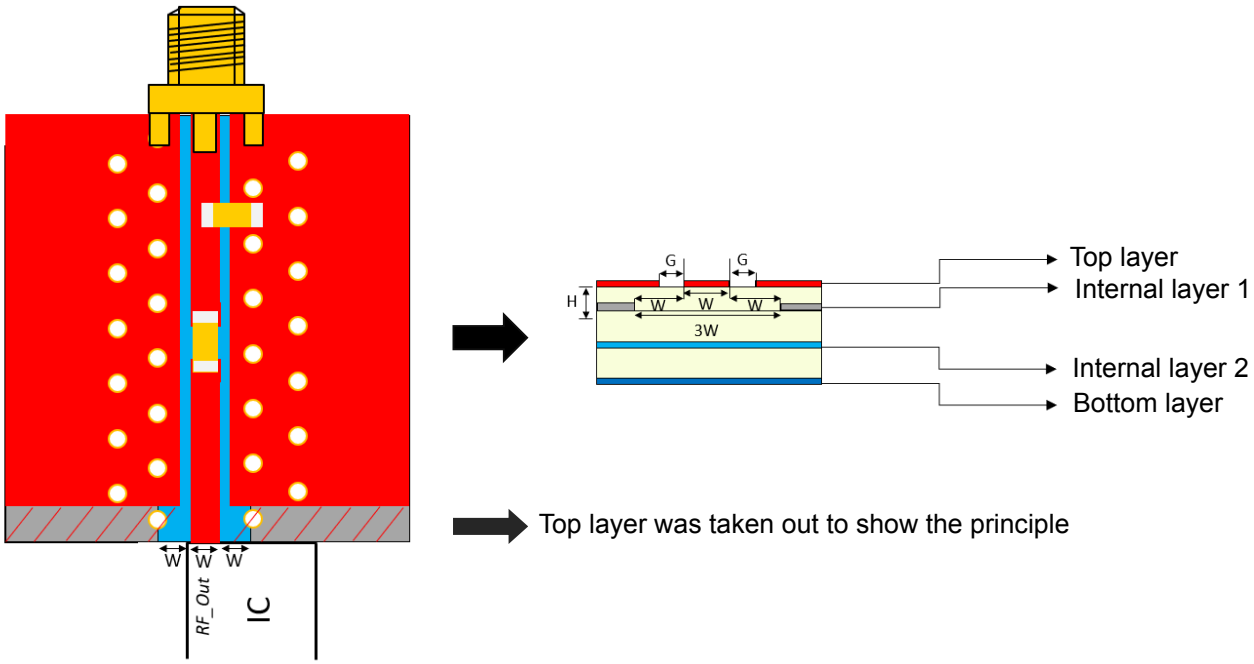


7 Cutout

Metal cutout is needed sometimes to have 50 Ω impedance in RF lines. If needed, make a cut in the GND of 3W (W equals to the RF track width) in the internal layers.

Depending on the design, the cutout could be needed in one or more layers. Speak with the PCB supplier or use RF simulation software to know if the cutout is necessary.

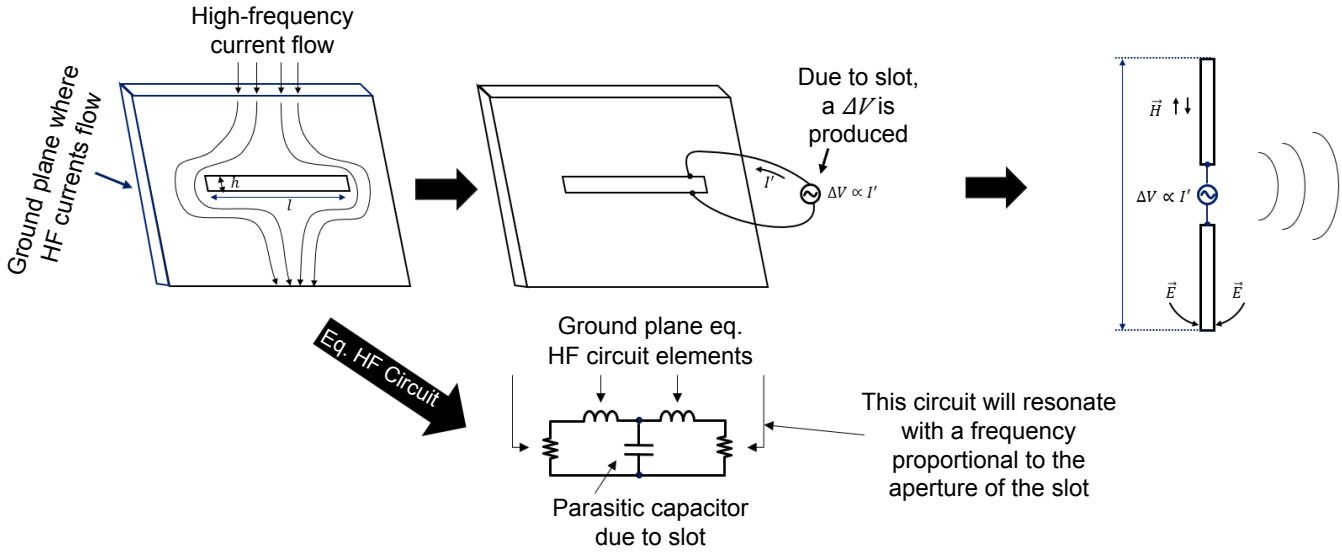
Figure 15. PCB cutout for 50 Ω impedance



8 Slots and high-frequency currents

Due to time-varying characteristics of RF currents, slots can act like antennas:

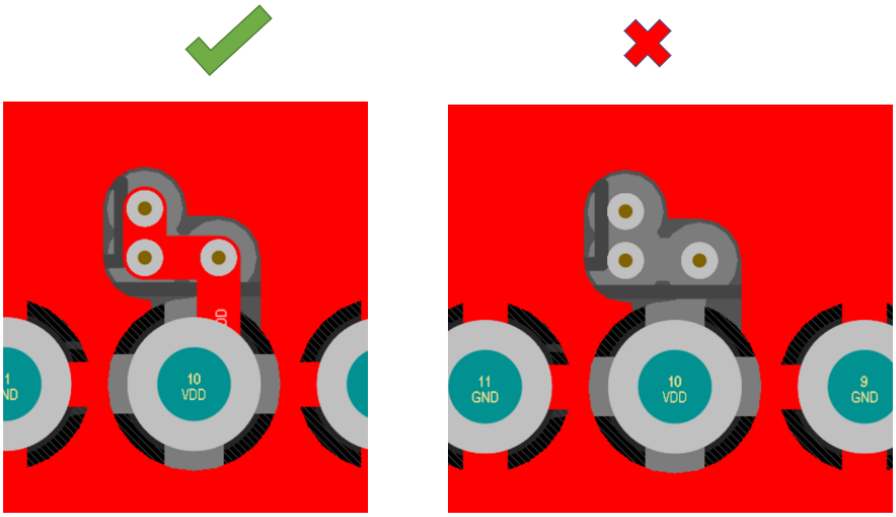
Figure 16. Slots and high-frequency currents



Here are some tips to avoid slots in your design:

- Try to avoid slots. If it is not possible, put some vias connected with a trace to minimize the slot.

Figure 17. Slot reduction with track



- Try to group vias to avoid creating any gap.

Figure 18. Slot reduction through spacing vias

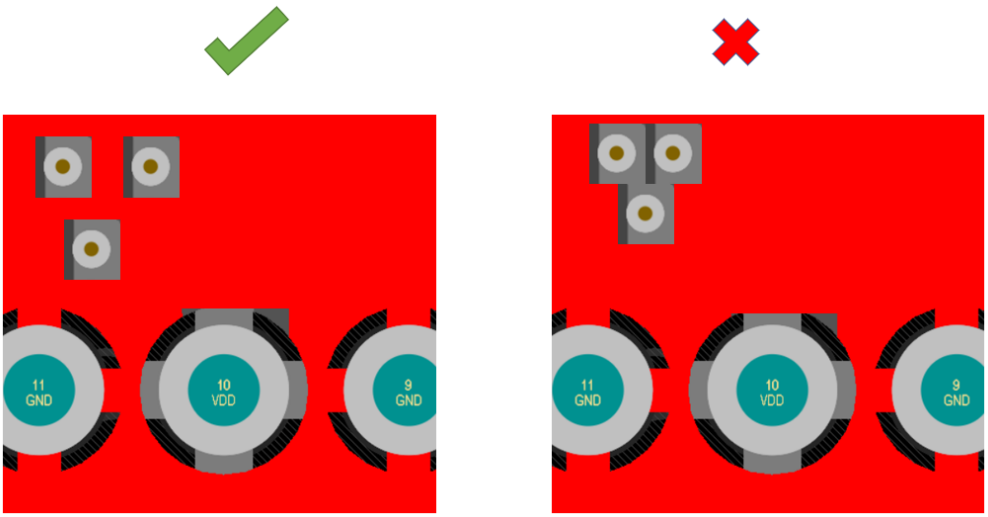
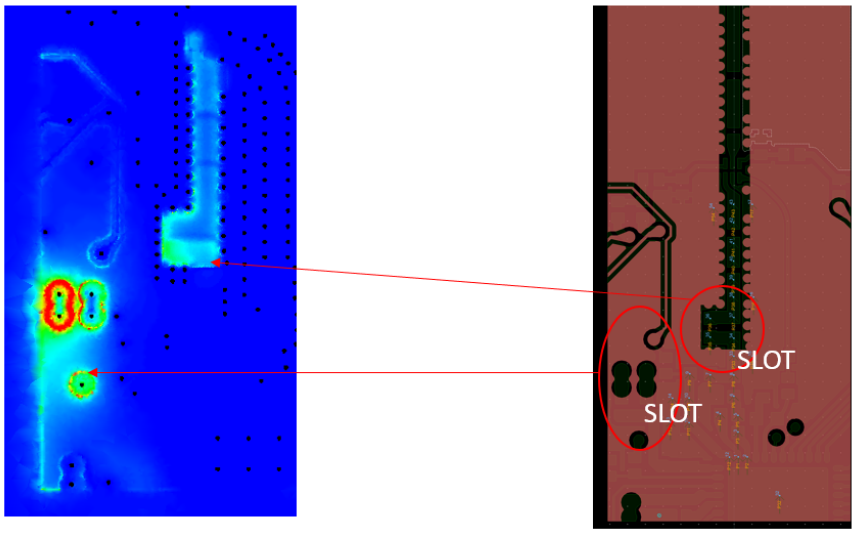


Figure 19. Effect of slots in PCB through electromagnetic simulation



9 Discontinuities to avoid in transmission lines

When designing transmission line on PCB with a controlled impedance (50 Ω), the objective is to maintain the same impedance in the whole system in order to transfer as much as energy as possible to the antenna and to minimize the unintentional loss of energy in the transmission line.

Table 5. Layout discontinuities

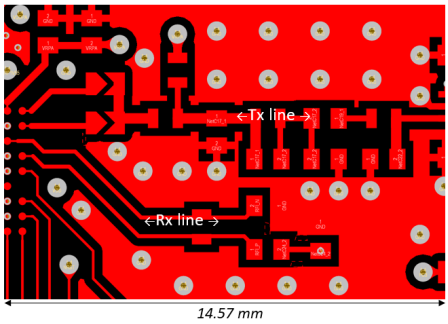
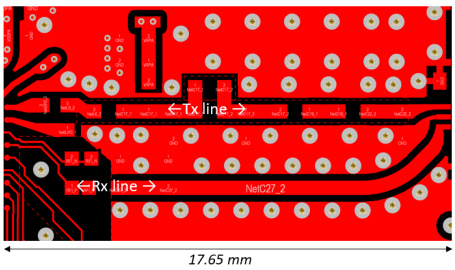
Performance	Layout	Comment
Poor		Difference between component pad widths and RF line widths, thermal reliefs and components placed in a way creating parasitic effects
Taking the above routing and increase slightly layout dimensions allow the user to route the RF lines without discontinuities as shown below.		
Recommended		Clean RF lines with pad components at the same width as the RF lines and pad components on the RF lines

Table 6. Track transitions

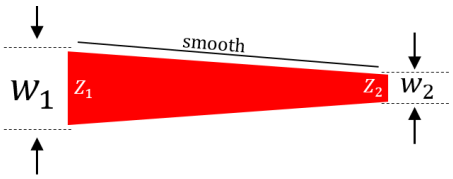
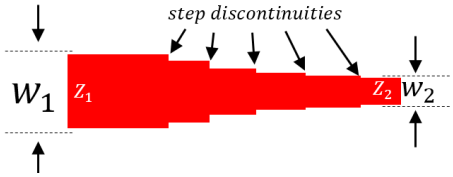
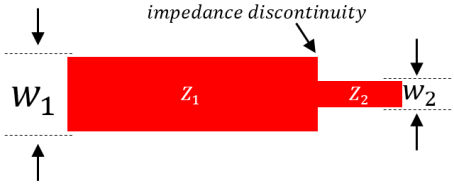
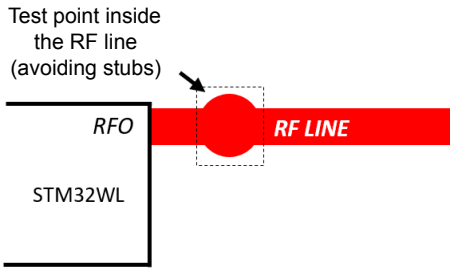
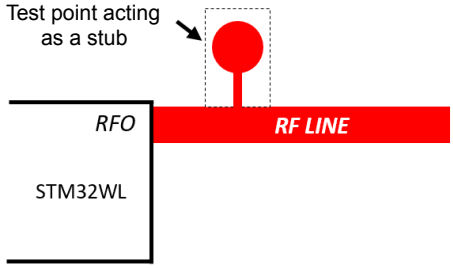
Performance	Transition type	Comment
Recommended		Smooth transition
Poor		Multi-step transition
Not good		Single-step transition

Table 7. Test points

Performance	Test point type	Comment
Recommended		Test point with **no** stub
Not good		Test point as stub

Whenever possible, align the width between the RF lines and pads (no transition needed). Do not hesitate to reduce pad components to maintain constant width of RF traces.

Table 8. Pad component width

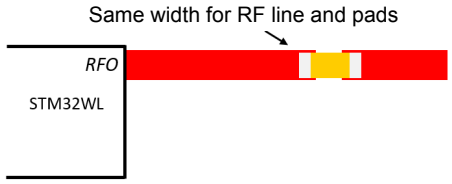
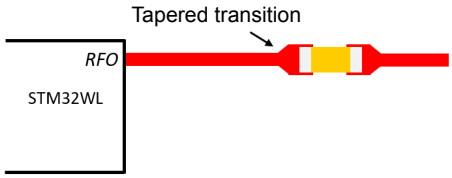
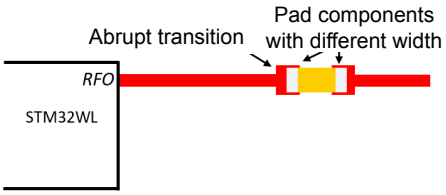
Performance	Pad component type	Comment
Recommended		**No** transition needed
Better		Smooth transition
Not good		Single-step transition

Table 9. RF switch transitions

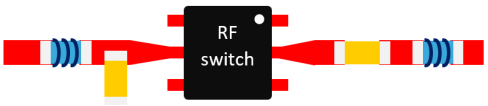
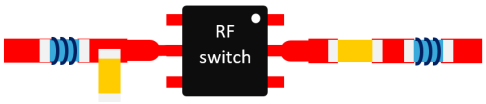
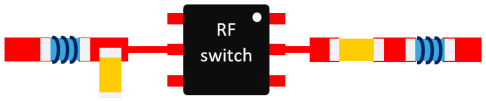
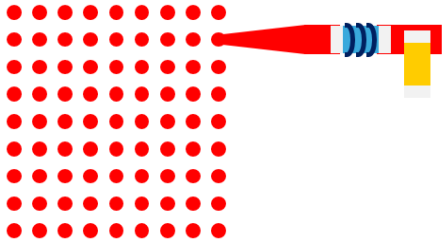
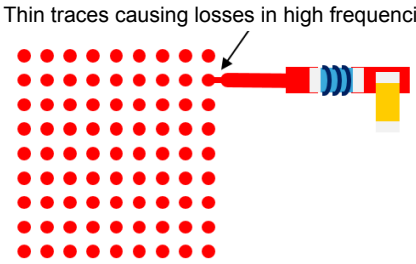
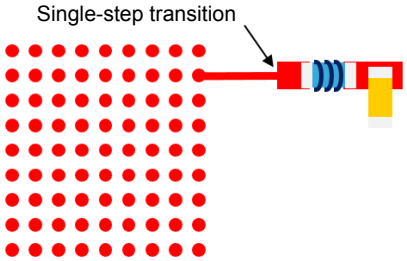
Performance	RF switch transition type	Comment
Recommended		Smooth transition
Better		Tapered transition
Not good		Single-step transition

Table 10. Package pad to RF line transitions

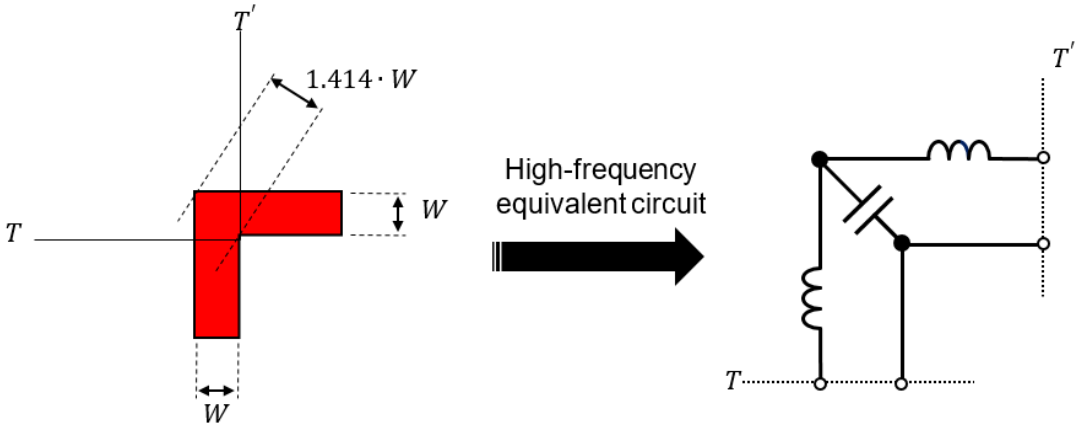
Performance	Pad to RF line transition type	Comment
Recommended		Smooth transition with polygons
Not good		Thin trace with single-step transition
		Single-step transition

10 Bends with RF lines

A bend is needed when there is a direction change for an RF line. Bends with RF lines can cause reflections and power loss. Some guidelines are detailed in this section to avoid issues with bends in high-frequency transmission lines. The main idea when designing bends is to keep the same trace width in the corner.

Consider the worst case that is the 90° bend shown in the figure below.

Figure 20. 90° bend example



The ideal case is a straight line with a constant width as shown below.

Figure 21. Ideal case: straight line



Table 11. **Guidelines for bends in RF lines**

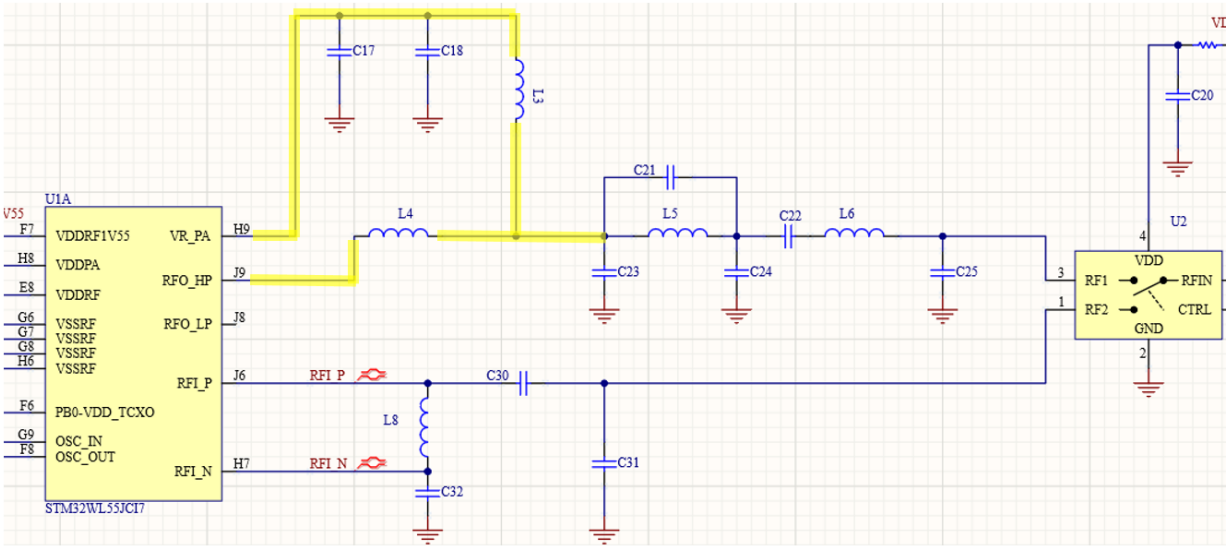
Performance	Bend type
Recommended	
Better	
Better	
Not good	

11 Minimize unintentional radiation

11.1 RFO harmonics

The typical RFO application circuit for the STM32WL is shown in the figure below.

Figure 22. Typical circuit for RFO harmonics



The STM32WL features a linear, high-efficiency RF PA (power amplifier) connected to the RFO pin (PA output). Due to the high-frequency harmonic components generated at RFO (above GHz for an operating frequency starting at 500 MHz), the RF tracks before filtering stages (before L5, C21, C24, C22, L6 and C25 in the schematic) may radiate unintentional electromagnetic (EM) energy. Any piece of metal that makes λ/4 under certain conditions, can act as an antenna radiating EM energy.

Note: Remember that the power radiated by a linear antenna of length L, is proportional to $P = (L/\lambda)^2$. This means that the bigger the unintentional antenna is, the greater the amount of energy it radiates.

The following formula can be used to determine the longest length of a track to not radiate EM energy on a PCB:

$$L < \frac{3 \times 10^8}{4 \times h \times f \times \sqrt{\epsilon_{r_eff}}}$$

where:

- h is the harmonic for which the user must determine the maximum track length to avoid.
- f is the operating frequency of the RF signal.
- ε_{r_eff} is the effective dielectric constant of the PCB stack-up layers.

Example

For an operating frequency at 915 MHz, the ninth harmonic (h9) is equal to 8.235 GHz (9 x 915 MHz). For PCB with an ε_{r_eff} = 3, the maximum track length is:

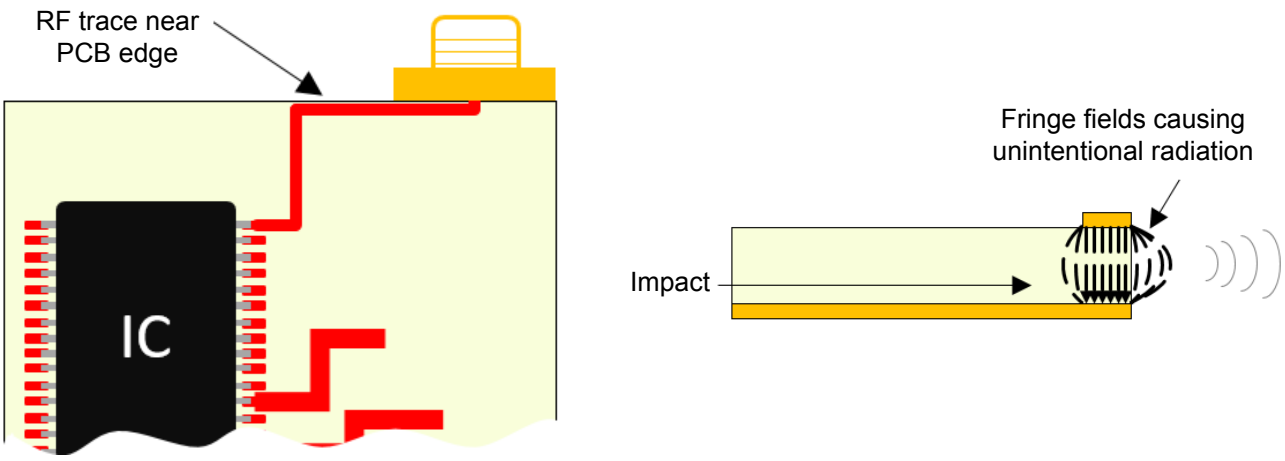
$$L < \frac{3 \times 10^8}{4 \times 9 \times 9.15 \times 10^6 \times \sqrt{3}}$$

The maximum track length to avoid an unintentional harmonic radiation with an operating frequency at 915 MHz and taking the ninth harmonic, is 5.258 mm.

11.2 High-frequency signals on board outline

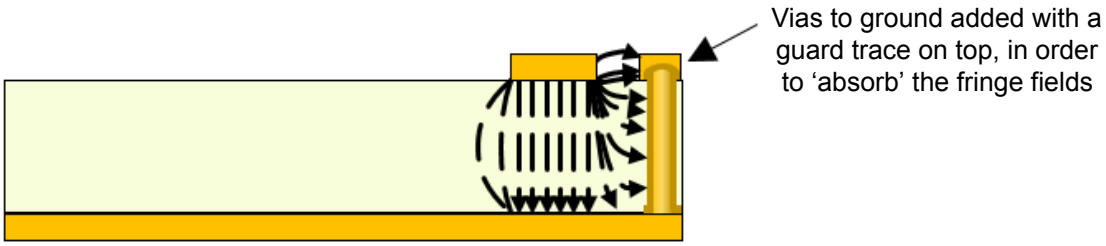
Routing high-frequency signals at board outline may cause unintentional EM radiation.

Figure 23. EM radiation generated by HF signals



One solution to mitigate the problem of tracks that radiate EM is to place them between grounded planes (below and above).

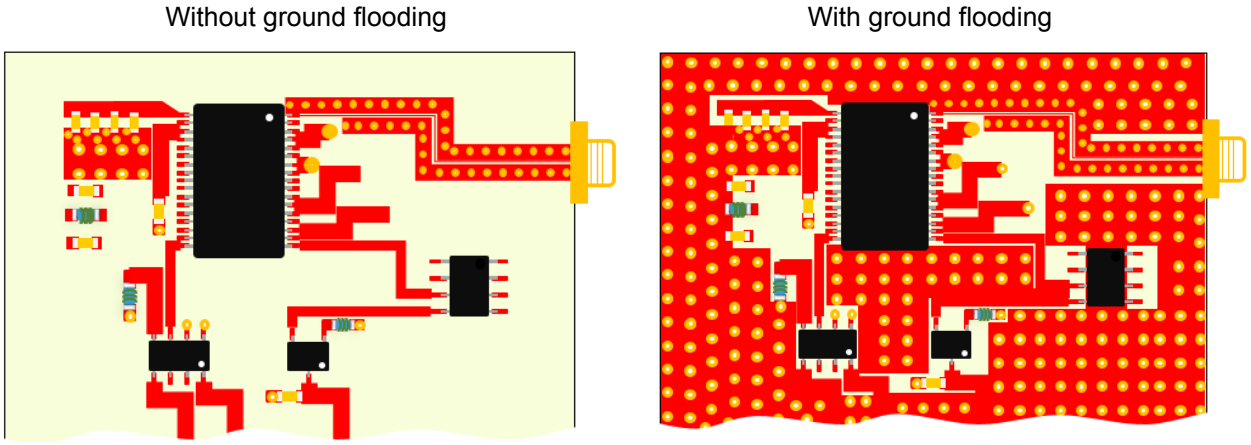
Figure 24. How to mitigate unintentional EM radiation



11.3 Ground flooding

Flooding unused PCB areas with GND and with multiple vias, can be used to keep the GND impedance low and reduce EMC issues.

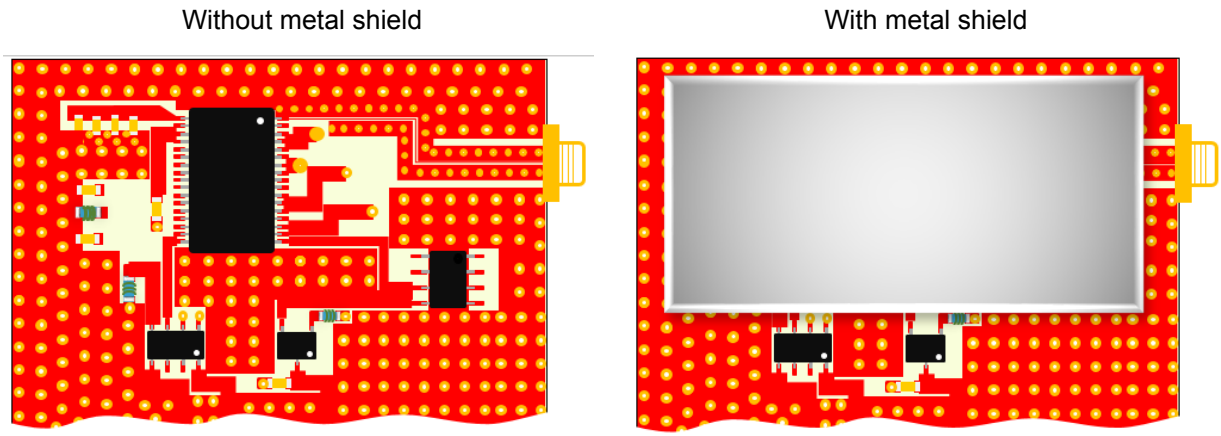
Figure 25. PCB example with or without ground flooding



11.4 Metal shield

To prevent issues due to unintentional radiation of harmonic contents, it is highly recommended to put a metal shield to cover the RF part on the board.

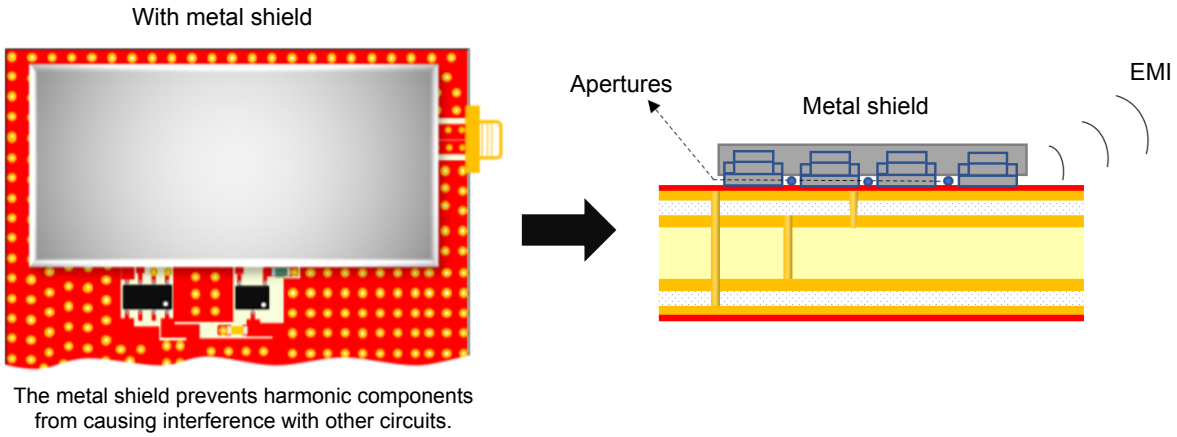
Figure 26. PCB example with or without metal shield



11.5 Shield apertures

When using a metal shield, be careful with the type of shield you are using since some shields have apertures in the connection part and these apertures can result in radiation leakage, or even worst act as antennas.

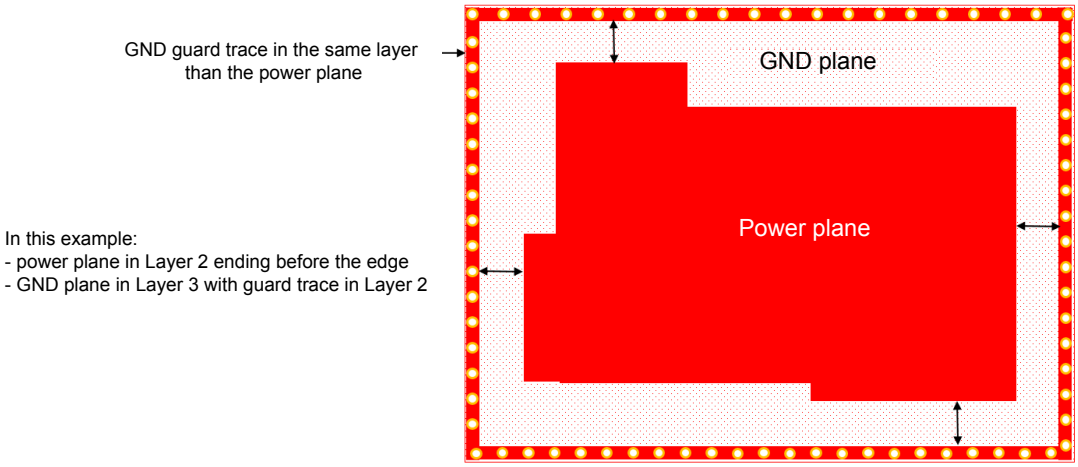
Figure 27. Aperture shield effect for electromagnetic emissions



11.6 Power planes and routing

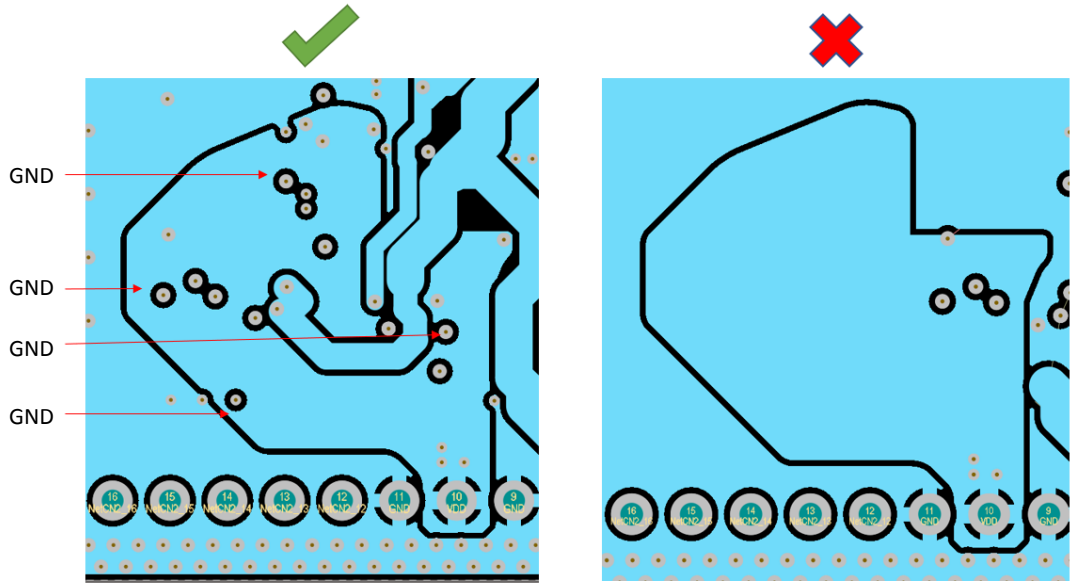
To prevent unintentional EM radiation between GND planes and power planes, the power planes must not be routed at the edge of the board. Otherwise, these power planes may radiate unintentional EM due to fringe fields. GND planes must be put in all layers around the board and must be connected.

Figure 28. GND and power planes



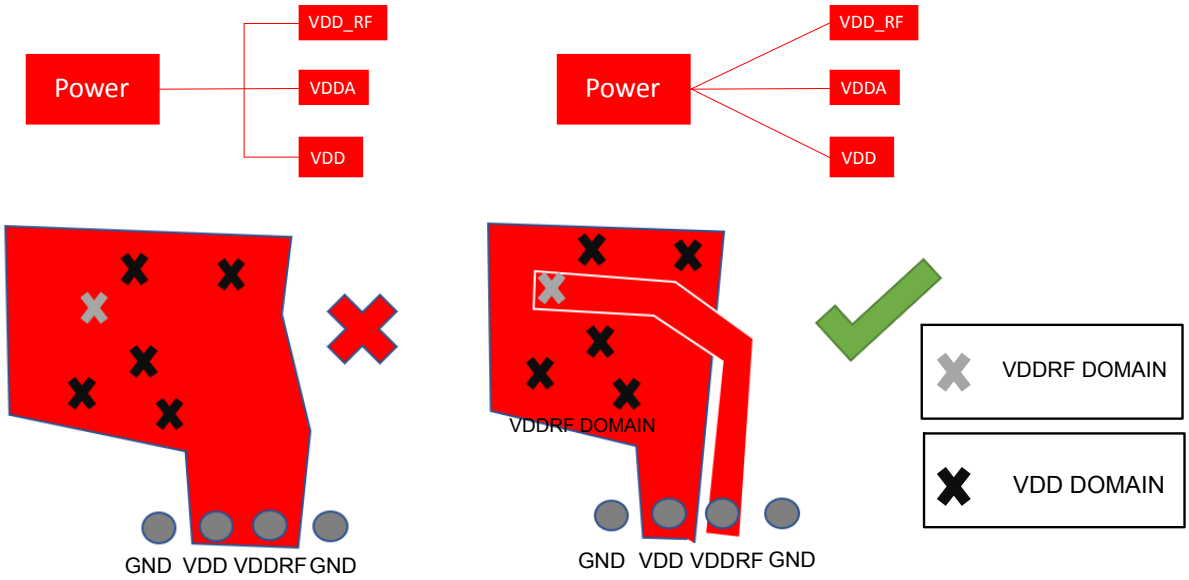
If you have a power plane in internal layers in your design, put some vias on it to avoid floating GND above and below ground planes. These vias should be distributed in the power plane.

Figure 29. GND vias on power plane to avoid floating GND



When routing power traces try to separate the main domains in star configuration, this is useful to avoid noise coupling and to measure correct current in a domain.

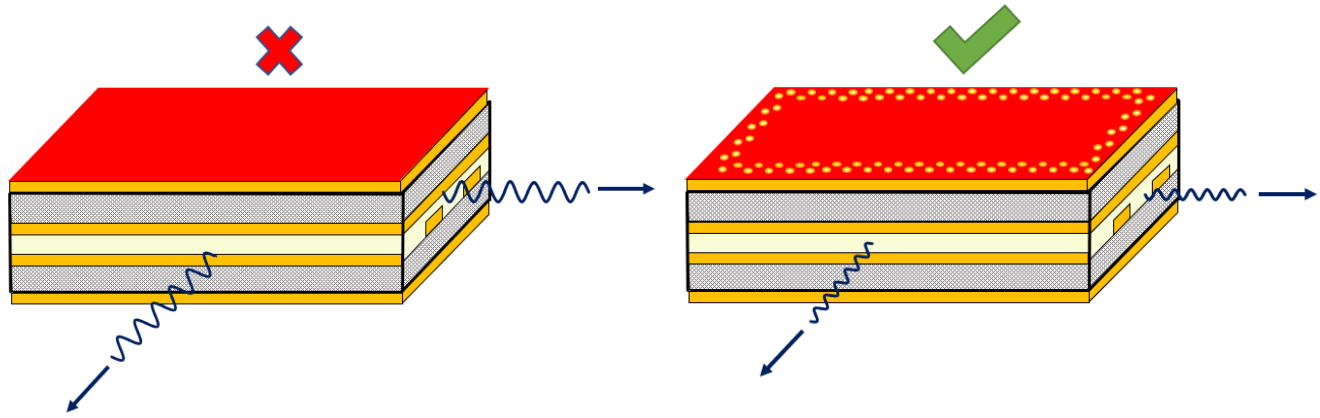
Figure 30. Routing different power domains to avoid noise problems



11.7 Via fencing

One of the main sources of EMI in PCB are the edges since we have a discontinuity in this part the electromagnetic waves that propagate between the coper and substrate of PCB can scape from this part of the board. Put some stitching vias in the edge and this should help to minimize EMI. A distance of λG/10 or less between vias should be used. See the reference layout for a real case application in Section 14 .

Figure 31. Effect of stitching vias in pcb edge to reduce emission



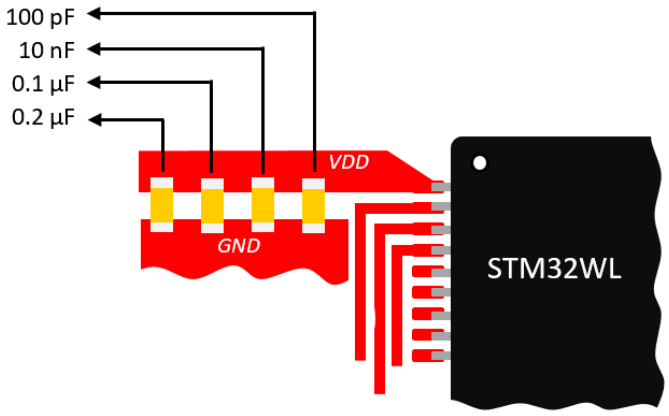
Unintentional radiation from board profile

Less radiation from board profile

12 Decoupling capacitors

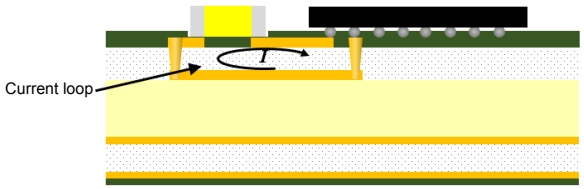
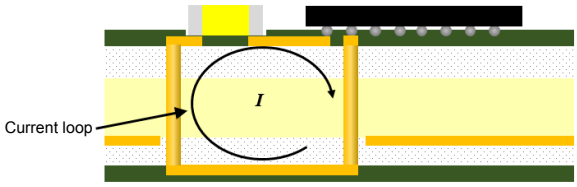
Capacitors with lower values must be placed closer to the chip than higher-value ones, as shown in the figure below.

Figure 32. Placement example of decoupling capacitors



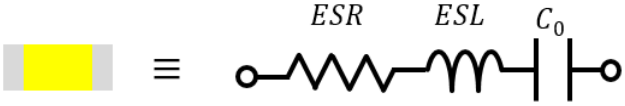
When routing decoupling capacitors, the smallest possible current loop must be maintained. Large current loops are translated into inductive behavior. Refer to AN5457 for more details on decoupling capacitors.

Table 12. Return currents for decoupling capacitors

Performance	Current loop of decoupling capacitors	Comment
Recommended		Reduced current loop
Poor		Large current loop

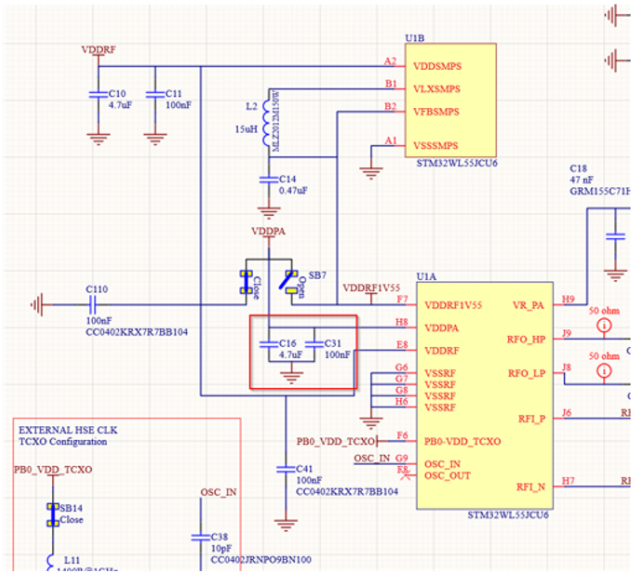
The equivalent series inductance (ESL, see the figure below) of a capacitor is impacted by the current loop.

Figure 33. High-frequency equivalent model of a capacitor



When using VDDSMPS in STM32WL, it is not recommended to use large decoupling capacitors on VDDPA. This is to avoid any voltage peak during SMPS operation. To address this issue, disconnect the 4.7 µF capacitor as shown in the figure below:

Figure 34. Decoupling capacitors in VDDPA



13 TCXO and XO considerations for PCB implementation with STM32WL

Depending on the RF output power, a special care must be made for the choice of crystals.

For STM32WL, three output powers are available:

- 22 dBm
- 17 dBm
- 14 dBm

Temperature-compensated oscillators (TCXO) and XO crystal are used as HSE (high-speed external) clock. They are essential for the good functioning of the RF circuit.

When the circuit is turn on, the RF output power generates heat that propagates in the PCB, affecting the precision of the crystal. This generates a frequency drift in the RF signal during a specific time. To avoid this effect, it is recommended to use TCXO crystal.

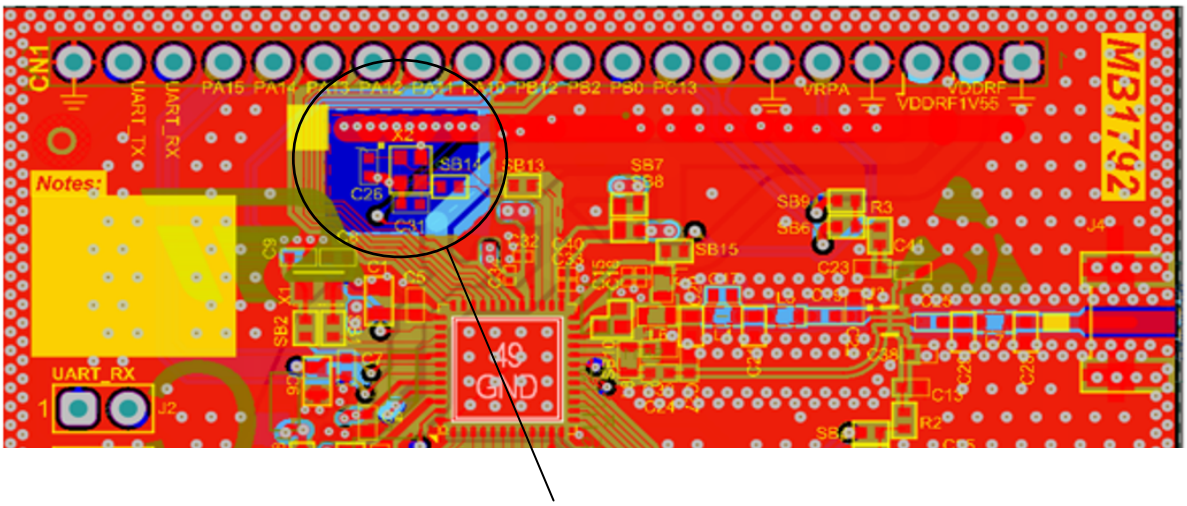
For designs with 22 dBm, the output power TCXO is needed.

For designs with 17 dBm and 14 dBm output powers, the TCXO is recommended. If it is not possible, a layout with thermal barrier must be done to minimize the frequency drift.

Warning: *Make sure that the slots do not work as antennas.*

See the example below:

Figure 35. Example of thermal barrier

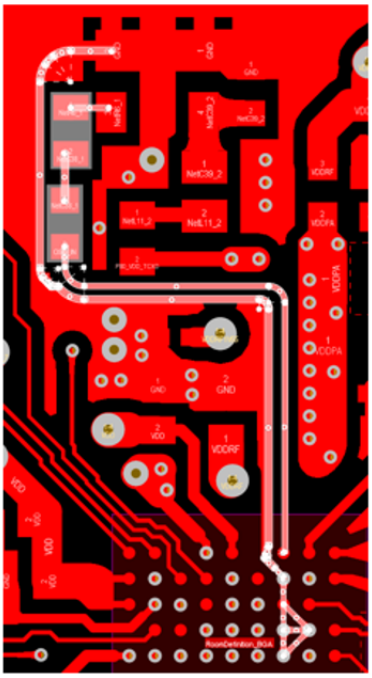


Thermal barrier cutout

When routing the crystal part, it is recommended to have a close loop and place the crystal as close as possible to the STM32WL, for a good performance.

See the example below:

Figure 36. Example of routing a crystal



14 STM32WL reference layout

The reference PCB 4-layer layout for BGA package is detailed in the figures below.

Figure 37. All layers of STM32WL reference layout for BGA

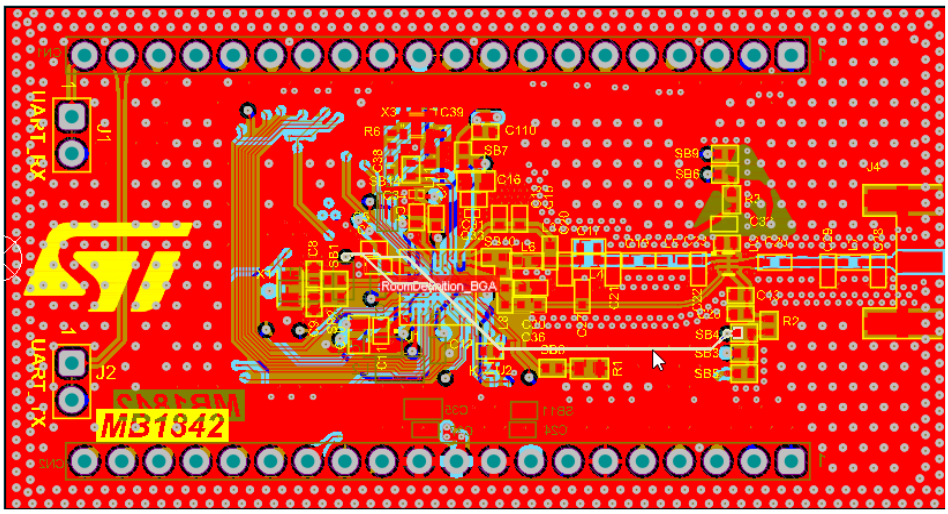


Figure 38. Top layer of STM32WL reference layout for BGA

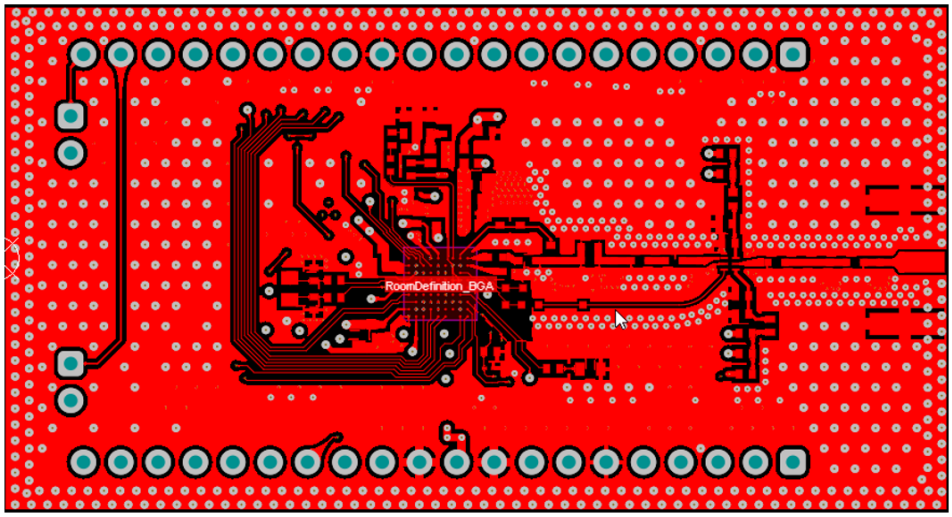


Figure 39. Middle layer 1 of STM32WL reference layout for BGA

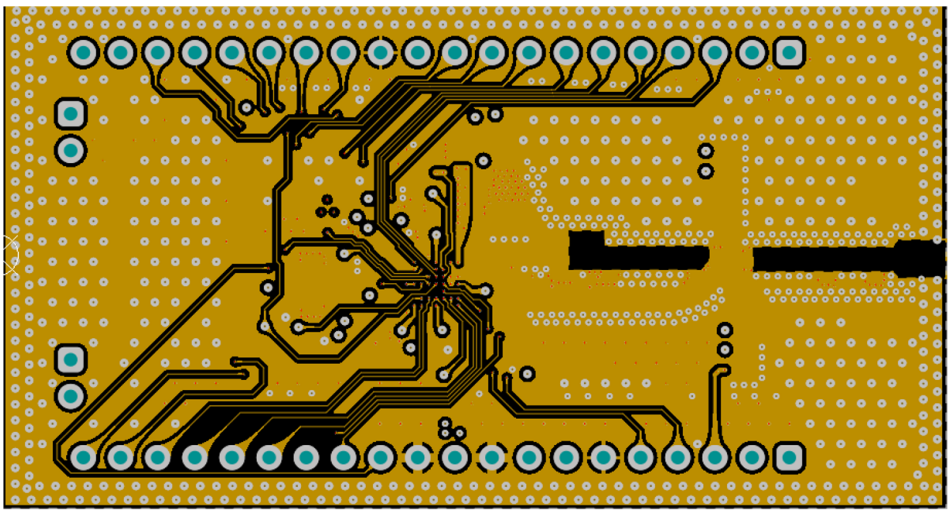


Figure 40. Middle layer 2 of STM32WL reference layout for BGA

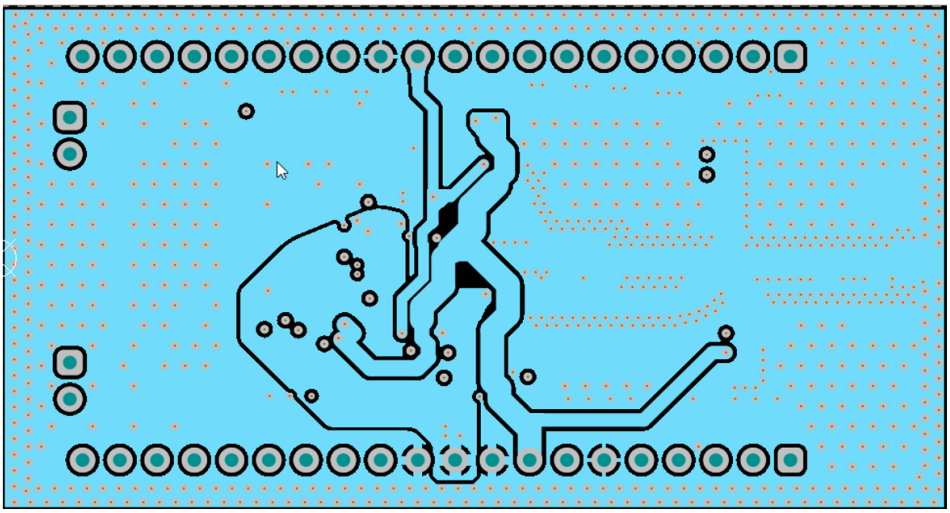
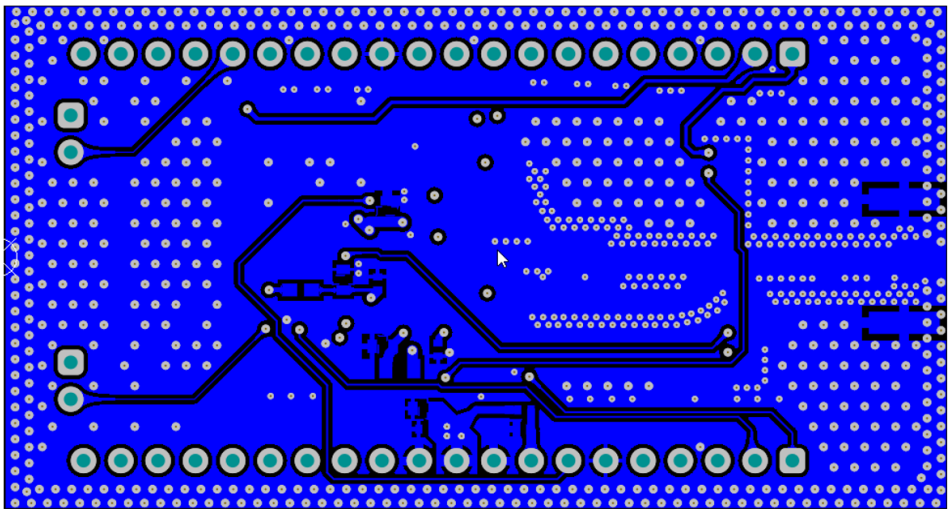


Figure 41. Bottom layer of STM32WL reference layout for BGA



The reference PCB 4-layer layout for QFN package is detailed in the figures below.

Figure 42. All layers of STM32WL reference layout for QFN

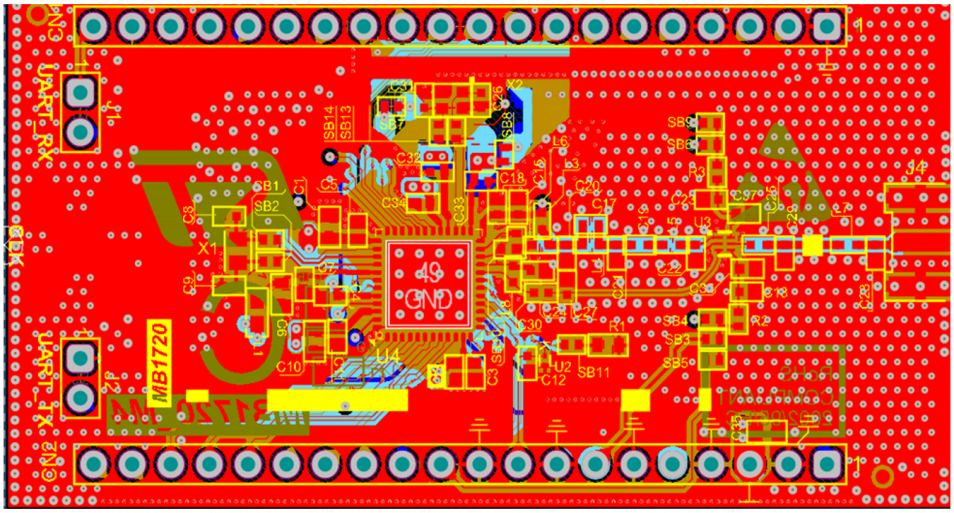


Figure 43. Top layer of STM32WL reference layout for QFN

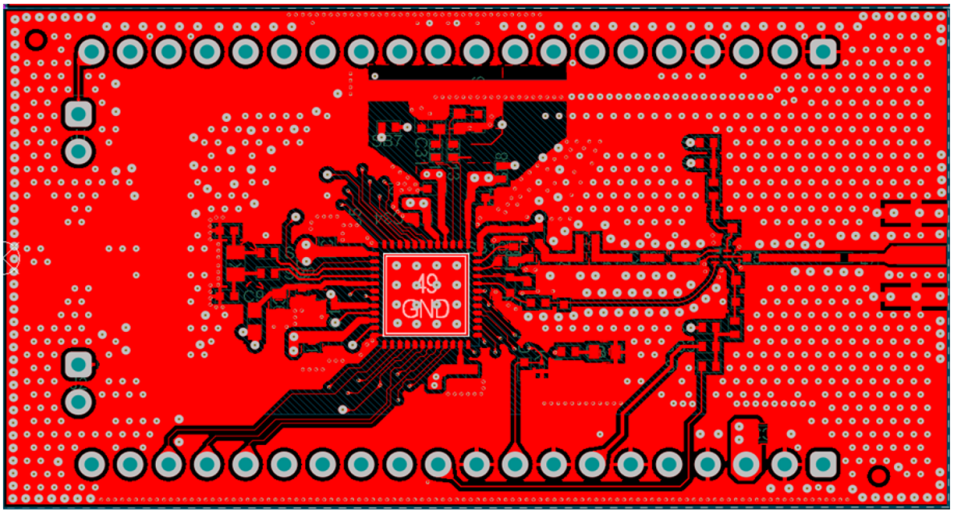


Figure 44. **Middle layer 1 of STM32WL reference layout for QFN**

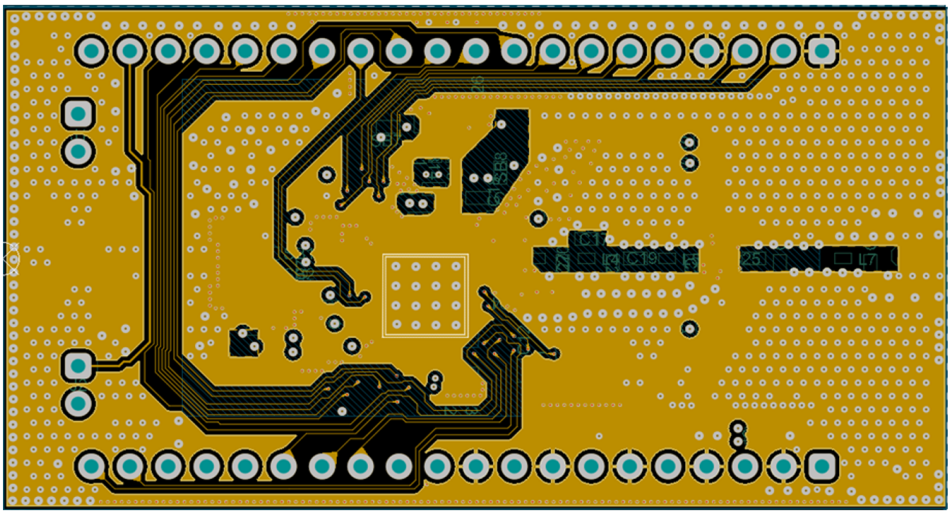


Figure 45. **Middle layer 2 of STM32WL reference layout for QFN**

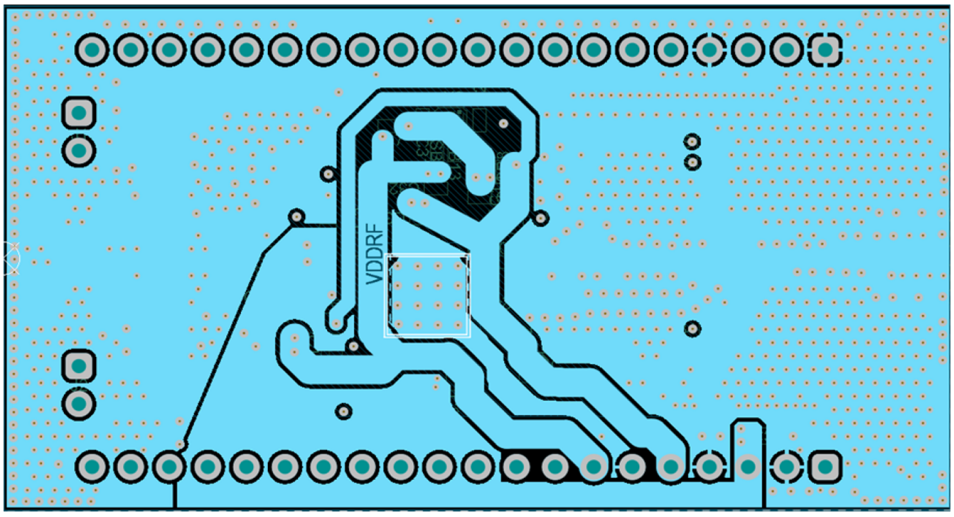
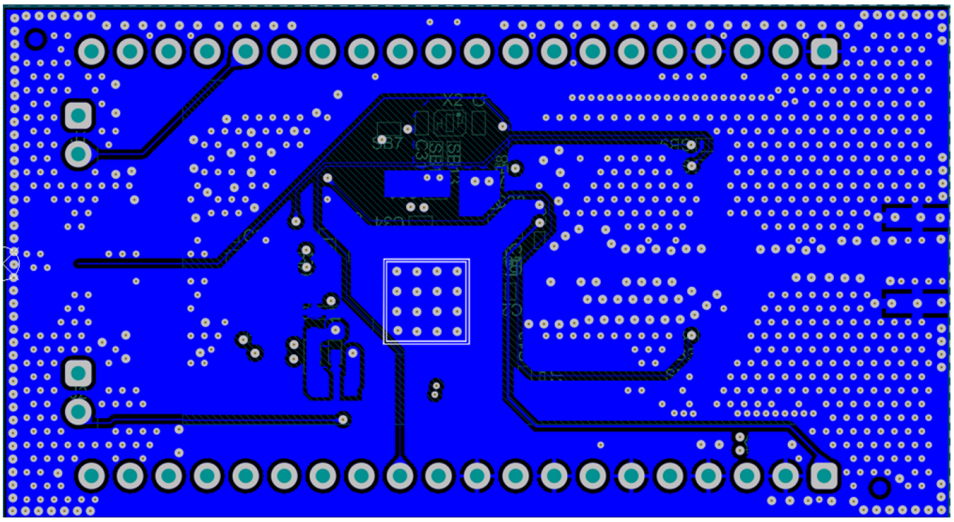


Figure 46. **Bottom layer of STM32WL reference layout for QFN**



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16 Conclusion

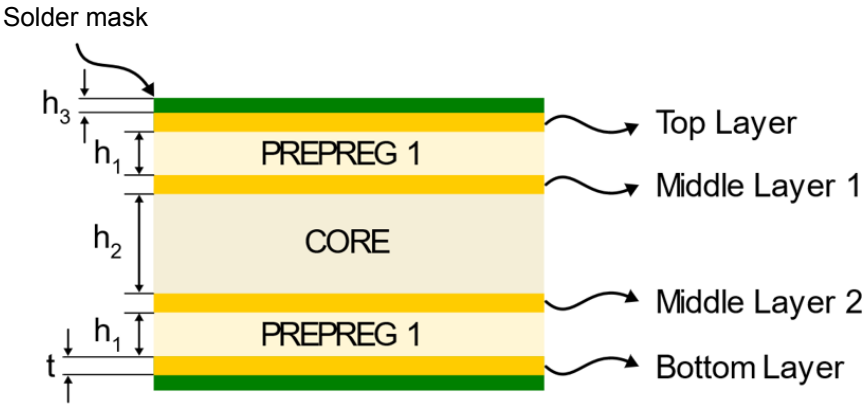
Some care must be taken when designing an RF board. Guidelines for decoupling capacitors, RF general rules, reduction of EMC issues, controlled impedances with predefined PCB stack-up layers are presented in this application note. The user must adapt these guidelines to the application.

Those guidelines must be followed to secure a correct behavior of the application, with high performance for the RF part of the STM32WL board.

Appendix A Stack-up examples

Some stack-up examples to obtain 50 Ω for Tx lines and 100 Ω for Rx lines from a typical stack-up for BGA package as shown in the figure below.

Figure 47. Typical stack-up for BGA package



- **Case 1**: typical stack-up for BGA package with **PCB total thickness = 1.04 mm**
  Consider configuration detailed in the table below.

Table 13. Case 1: PCB total thickness = 1.04 mm

Dielectric materials				Metal layers	
Element	**Material**	**Nominal thickness h_x (µm)**	**ε_r**	**Layer**	**Nominal thickness t (µm)**
Solder mask (h_3)	Solder resist	20	3.7	Top	35
Prepreg 1 (h_1)	1 x 2116	70	3.5	Middle 1 and middle 2	35
Core (h_2)	FR4	710	5.0	Bottom	35

The Tx and Rx lines detailed in the figures below can then be built from this configuration.

Figure 48. Tx 50 ohms RF tracks (case 1, PCB total = 1.04 mm)

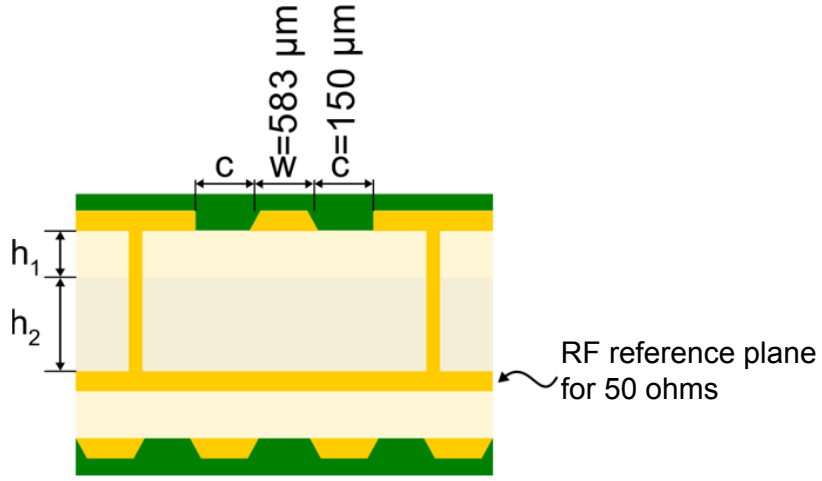
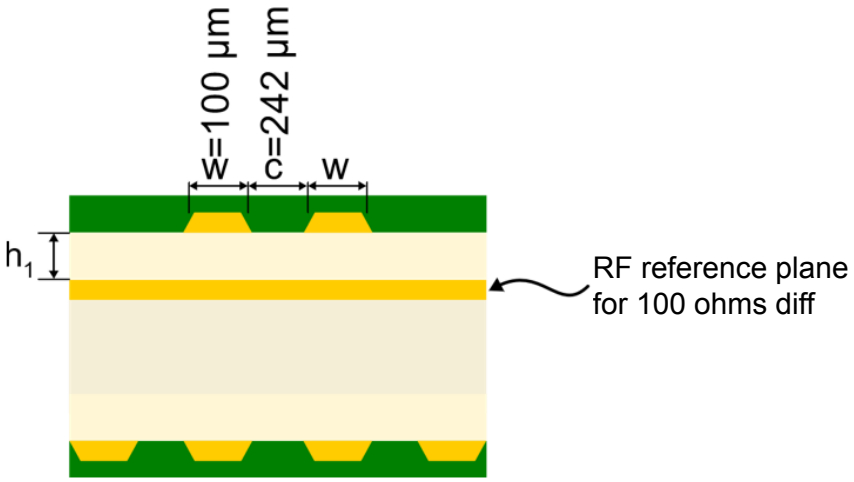


Figure 49. Rx 100 ohms differential pair (case 1, PCB total = 1.04 mm)



- **Case 2**: typical stack-up for BGA package with **PCB total thickness = 1.10 mm**
  Consider configuration detailed in the table below.

Table 14. Case 2: PCB total thickness = 1.10 mm

Dielectric materials				Metal layers	
Element	**Material**	**Nominal thickness h_x (µm)**	**ε_r**	**Layer**	**Nominal thickness t (µm)**
Solder mask (h_3)	solder resist	20	3.3	Top	35
Prepreg 1 (h_1)	1 x 2116	108	3.8	Middle 1 and middle 2	35
Core (h_2)	FR4	710	5.0	Bottom	35

The Tx and Rx lines detailed in the figures below can then be built from this configuration.

Figure 50. Tx 50 Ω RF tracks (case 2, PCB total = 1.10 mm)

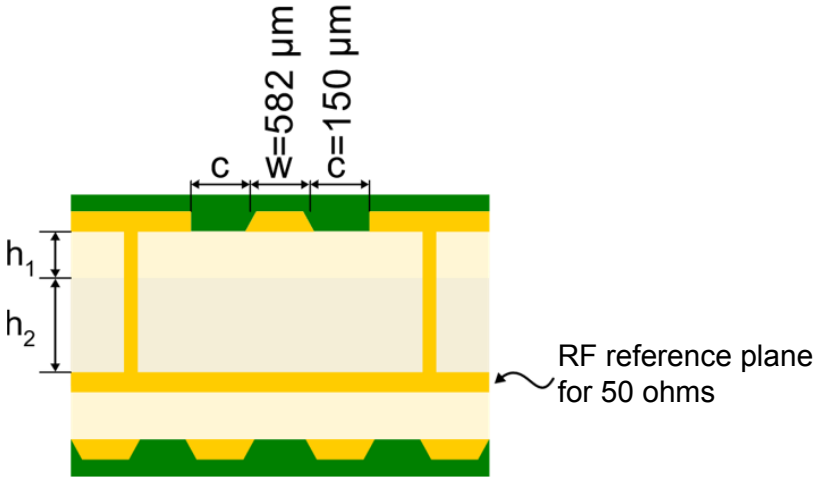
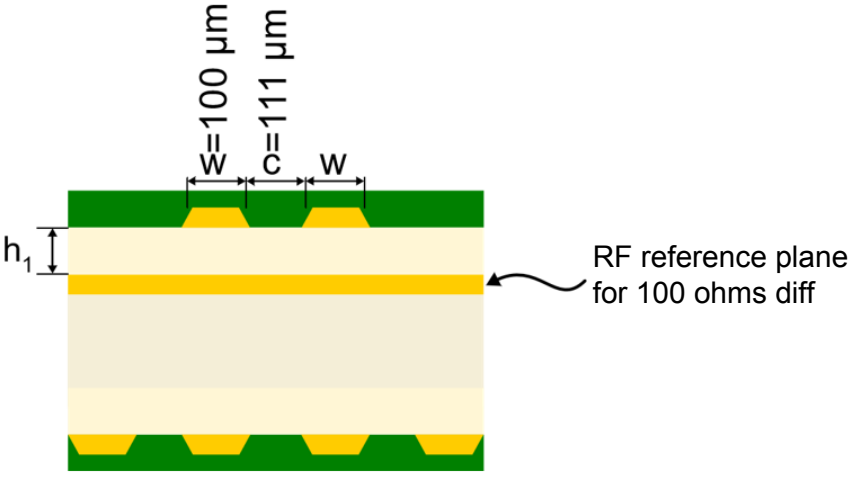


Figure 51. Rx 100 Ω differential pair (case 2, PCB total = 1.10 mm)



- **Case 3**: typical stack-up for BGA package with **PCB total thickness = 1.60 mm**
  Consider configuration detailed in the table below.

Table 15. Case 3: PCB total thickness = 1.60 mm

Dielectric materials				Metal layers	
Element	**Material**	**Nominal thickness h_x (µm)**	**ε_r**	**Layer**	**Nominal thickness t (µm)**
Solder mask (h_3)	solder resist	20	3.5	Top	35
Prepreg 1 (h_1)	1 x 1080	76	4.18	Middle 1and 2	35
Core (h_2)	7 x 7628	1268	4.74	Bottom	35

The Tx and Rx lines details in the figures below can then be built from this configuration.

Figure 52. Tx 50 Ω RF tracks (case 3, PCB total = 1.60 mm)

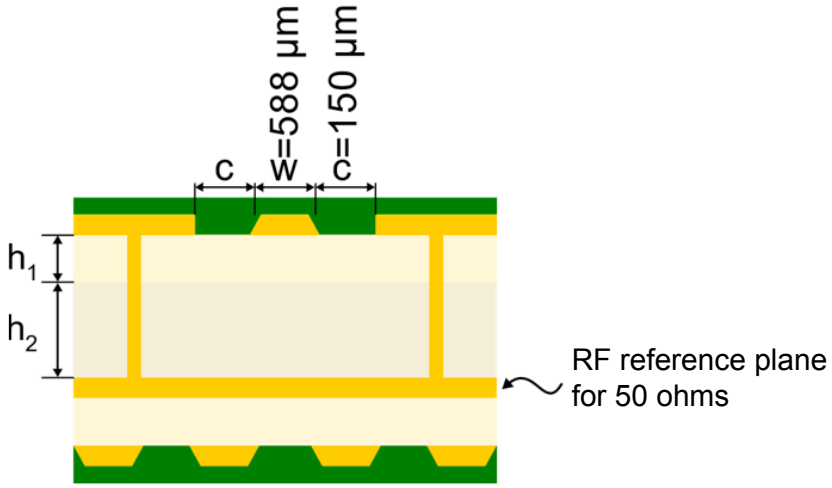
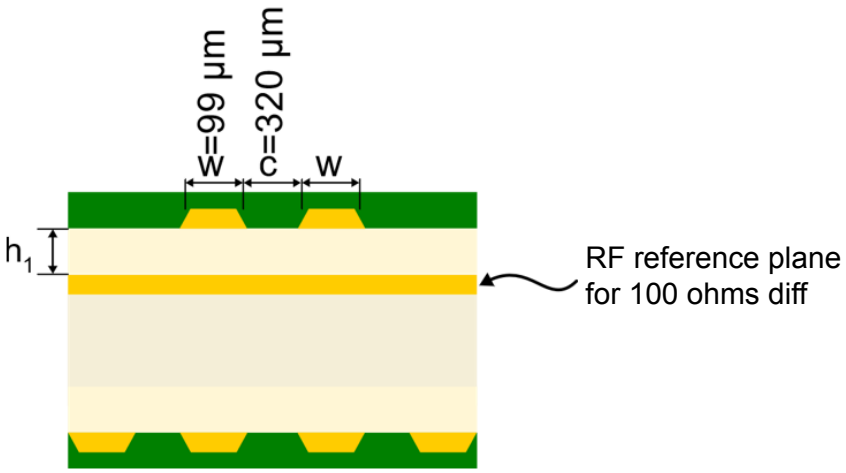


Figure 53. Rx 100 Ω differential pair (case 3, PCB total = 1.60 mm)



Important: The longer the distance is between the source and the antenna, the greater the potential for loss of energy in the RF transmission line. As a design rule, RF transmission lines must be as short as possible and without discontinuities.

Revision history

Table 16. **Document revision history**

Date	Version	Changes
6-Mar-2020	1	Initial release.
10-Jul-2020	2	Removed section 3.3 Metal cutout for impedance control.
15-Apr-2022	3	Updated: • Section 2 Characteristic and controlled impedance • Section 4.1 Capacitors • Section 5 Via stitching and shielding • Section 6 RF return current path • Section 12 Decoupling capacitors • Section 14 STM32WL reference layout Added: • Section 7 Cutout • Section 8 Slots and high-frequency currents • Section 11.5 Shield apertures • Section 11.7 Via fencing • Section 13 TCXO and XO considerations for PCB implementation with STM32WL

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